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Development of a low-noise analog front-end ASIC for CdTe detectors

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Abstract

This paper describes the recent development of a low-noise analog front-end ASIC for CdTe detectors. The ASIC is designed on the basis of the Open-IP LSI project led by JAXA and implemented using TSMC 0.35-μm CMOS technology. The ASIC contains eight identical channels, each of which includes a charge-sensitive amplifier, band-pass filters, and a sample-and-hold circuit. Preliminary testing of the ASIC achieved noise performance of $188e^- + 7.5e^-/pF$. In order to verify the low-noise characteristics, the ASIC was connected to a guard-ring-equipped CdTe diode detector with dimensions of 2.4 × 2.4 mm and having a thickness of 0.5 mm. As a result, the gamma-ray spectra of radioactive sources were obtained with good energy resolutions of 2.51 and 2.35 keV (FWHM) for gamma rays of 59.5 and 122 keV, respectively, at room temperature.
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1. Introduction

One of the primary objectives of future X-ray missions is to explore the universe with very high sensitivity in the 10–100 keV band, where nonthermal emission becomes dominant over thermal emission. This exploration could be achieved by employing a multilayer, grazing incidence hard X-ray telescope ("super mirror") in conjunction with a hard X-ray imaging detector used as a focal plane detector [1–3]. The detector system would require a high energy resolution of better than 1 keV (Full-Width-at-Half-Maximum or FWHM) at 60 keV and a spatial resolution of better than 200 μm. Cadmium telluride (CdTe) has been considered a promising semiconductor material for focal detector systems, given its high stopping power of X-rays and gamma rays. Significant progress has been made in crystal growth technology to enable the development of large-area detectors, with good energy resolutions being reported in combination with several low-noise ASICs [4–8].

In the past few years, we have been working on the development of low-noise analog ASICs for gamma-ray detectors; specifically, one-dimensional ASICs [9] and two-dimensional ASICs [10]. The one-dimensional ASICs have relatively simple circuits and the main objective is to construct a set of verified designs of circuit blocks to be used for signal processing in radiation detectors. Conversely, the two-dimensional ASICs were developed for the hybrid pixel imaging detector to be used in the hard X-ray and gamma-ray observations in space. Both ASICs have reached a noise level of less than $300e^-$, although practical use requires further improvement of noise performance.

To achieve ASICs of even lower noise, we have newly developed a one-dimensional, eight-channel, low-noise analog ASIC designated the "KW01". The main objective

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here is to demonstrate the newly designed circuit blocks and establish a low-noise architecture. All circuit architectures are based on the Open-IP LSI project led by JAXA [9–11]. Since Open-IP consists of reusable circuit blocks extracted from our ASIC designs, the circuit library is flexibly updated with and applicable to the further development of low-noise two-dimensional ASICs.

This paper presents the design and initial performance of the KW01 chip. Section 2 describes the basic structure of the KW01 and details the circuit schematics. The ASIC employs a newly designed high-impedance circuit instead of an FET used as a transfer gate for a feedback component, as is often used in several low-noise ASICs [12–18]. Section 3 presents the setup of the performance measurements. Section 4 gives the preliminary experimental results of ASIC performance. Section 5 reports on the spectral performance in combination with a CdTe diode detector. Finally, Section 6 gives a summary and conclusion.

2. Circuit description

2.1. Overview of the ASIC

The KW01 is implemented using TSMC 0.35-μm CMOS technology with such options as 4-metal, 2-poly, and mounted in a plastic-mold package. Fig. 1 shows a photograph of the ASIC. The chip size is 2.95 × 2.95 mm with eight readout channels, and has total power consumption of 33 mW for the power rails of ±1.65 V. There exists some penalty on the power consumption to improve the dynamic range. The buffer circuits equipped for monitoring analog signals also contribute additional power dissipation. In order to mitigate interference between the analog and digital circuits, special care was taken for the layout as follows: (a) the area surrounding the entire chip is separated between the analog and digital circuits, (b) the digital circuits are concentrated on the right side of the chip and analog signals are processed in the left-to-right direction, and (c) bias and reference voltages are supplied from the top and bottom sides of the chip. Table 1 lists an overview of the ASIC.

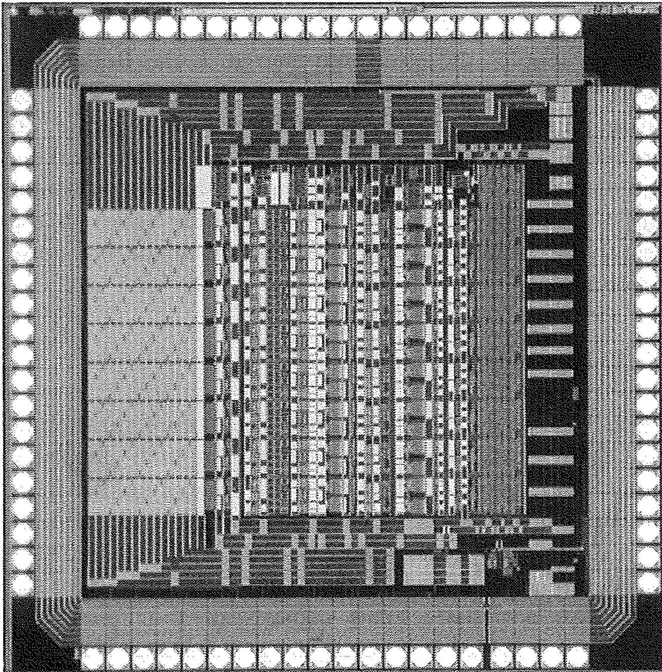

Fig. 1. Photograph of the KW01. Pads on the right and the bottom-right sides are for the digital circuits, and the others for analog circuits. Inputs for injected charge are on the left, with analog signals processed in the left-to-right direction. Output and monitor pads are on the top side. Bias voltages are supplied from both the top and bottom pads.

2.2. Analog processing

The analog circuit chain consists of a charge-sensitive amplifier (CSA), band-pass filters, comparator, and sample-and-hold circuit as shown in Fig. 2. CSA input is provided with an ESD protection circuit. A capacitor ($C_{in} = 0.1$ pF) is attached for test pulse injection. CSA output is split into two different filter circuits whose circuit architectures are identical except for the time constants. The faster circuit (with a peaking time of 1.5 μs) is fed into the comparator to generate a hit signal with an one-shot trigger circuit. The slower circuit (with a peaking time of 3 μs) is connected to the sample-and-hold circuit with a storage capacitor of $C_h = 0.8$ pF. Analog outputs for the eight readout channels are held simultaneously by a properly timed external signal and serially read out in a multiplexing scheme.

The transfer function of the CSA is given as

$$T_1(s) = -\frac{R_f}{1 + sC_fR_f} \tag{1}$$

where s denotes the complex angular frequency, R_f the feedback resistance, and C_f the feedback capacitance.

In order to focus on the basic properties of the circuit chain in the present ASIC, a pole-zero-cancellation circuit is not employed. Instead, we adopted a large decay-time constant of C_fR_f for the CSA and attempted to reduce the undershoot as well as decrease the contribution of shot noise.

Fig. 2 shows the filter circuit as a rectangle of dashed lines. The transfer function of the filter circuit is given as

$$T_2(s) = -\frac{sC_0R_1}{s^2C_1C_2R_1R_2 + sR_1C_1 + 1}. \tag{2}$$

Table 1
Overview of the KW01

Fabrication process	TSMC 0.35-μm CMOS
Options	4-metal, 2-poly
Chip size	2.95 × 2.95 mm^2
Number of channels	8
Total power consumption	33 mW
Power rail	±1.65 V

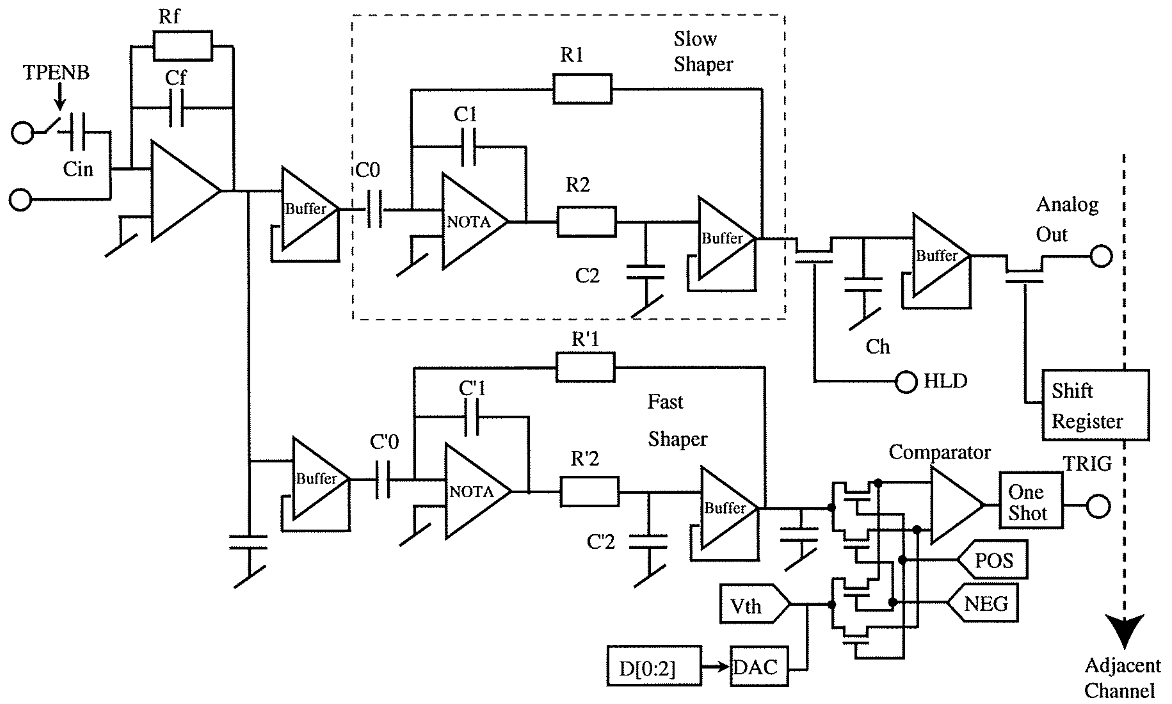

Fig. 2. Signal processing chain for each channel. Here, typical values of the capacitors and resistors are $C_{\rm in} = 0.1\,\rm pF$, $R_{\rm f} = 400\,\rm M\Omega$, $C_{\rm f} = 0.02/0.04\,\rm pF$, $C_0 = 3.2/6.4\,\rm pF$, $C_1 = C_2 = 0.5/1.0\,\rm pF$, $R_1 = R_1' = 6\,\rm M\Omega$, $C_0' = 0.66/1.32\,\rm pF$, $C_1' = C_2' = 0.1/0.2\,\rm pF$, $R_2 = R_2' = 1.5\,\rm M\Omega$, $C_{\rm h} = 0.8\,\rm pF$.

By setting the parameters as $C_1R_1 = 4C_2R_2$, the transfer function is reduced as

$$-\frac{sC_0R_1}{(2sC_2R_2+1)^2}. \tag{3}$$

This circuit has a degenerated pole at $s = -1/2C_2R_2$ and functions as a low-pass filter. Eventually the entire transfer function of the signal processing chain is given by $T_1(s)\cdot T_2(s)$, which yields

$$\frac{R_{\rm f}}{1+sC_{\rm f}R_{\rm f}}\cdot\frac{sC_0R_1}{(2sC_2R_2+1)^2}. \tag{4}$$

By assuming $C_{\rm f}R_{\rm f} \gg 1/|s|$, the zero of $T_2(s)$ compensates the pole of $T_1(s)$ and the transfer function is rewritten as

$$2\cdot\frac{C_0}{C_{\rm f}\cdot C_1}\cdot\frac{1/T_{\rm M}}{(s+1/T_{\rm M})^2} \tag{5}$$

where we employ the relation $T_{\rm M} = 2C_2R_2$. In case $C_{\rm f}R_{\rm f}$ is not negligible compared to $T_{\rm M}$, the transfer function is given as

$$2\cdot\frac{C_0}{C_{\rm f}\cdot C_1}\cdot\frac{1/T_{\rm M}}{(s+1/T_{\rm M})^2}\cdot\frac{s}{(s+1/C_{\rm f}R_{\rm f})}. \tag{6}$$

Should this be the case unlike in Eq. (5), undershoot occurs, although a high count rate is not required in space applications. Thus, the degradation of pulse height is thought to be sufficiently small.

As for the case of Eq. (5), the entire circuit functions as a CR-RC shaper and the equivalent noise charge is written as follows [19]:

$$Q_{\rm n}^2 = \left(\frac{e^2}{8}\right)\left[\left(2qI_{\rm d}+\frac{4kT}{R_{\rm p}}\right)\cdot T_{\rm M} + (4kTR_{\rm S})\cdot\frac{C_{\rm D}^2}{T_{\rm M}} + 4A_{\rm f}C_{\rm D}^2\right] \tag{7}$$

where q denotes the electronic charge, k the Boltzmann constant, T the absolute temperature, $I_{\rm d}$ the detector leakage current, $R_{\rm p}$ the input shunt resistance located in parallel with the detector capacitance $C_{\rm D}$, $T_{\rm M}$ the peaking time of the shaper, $R_{\rm S}$ ($= 2/3g_{\rm m}$ in the simplest presentation) the resistance equivalently located in series to the preamplifier input, and $A_{\rm f}$ the coefficient of the $1/f$ noise component.

2.3. Charge-sensitive amplifier

Fig. 3 shows the detailed CMOS circuit configuration of the CSA. The CSA consists of a preamplifier, feedback circuit, and feedback capacitor $C_{\rm f}$. The amplifier part consists of a folded cascode amplifier with a gain boost for the cascode transistor. Table 2 lists the dimensions of the PMOS input transistor and the main characteristics of the CSA. The feedback circuit consists of four p-channel transistors operated in a weak-inversion mode where the source drain current is linear with respect to the difference between the gate voltages of M2 and M5 (in Fig. 3). The impedance is equivalent to the total transconductance of M2 to M5 and the effective impedance of $R_{\rm f}$ is about 400 MΩ. These circuit blocks were commonly employed in

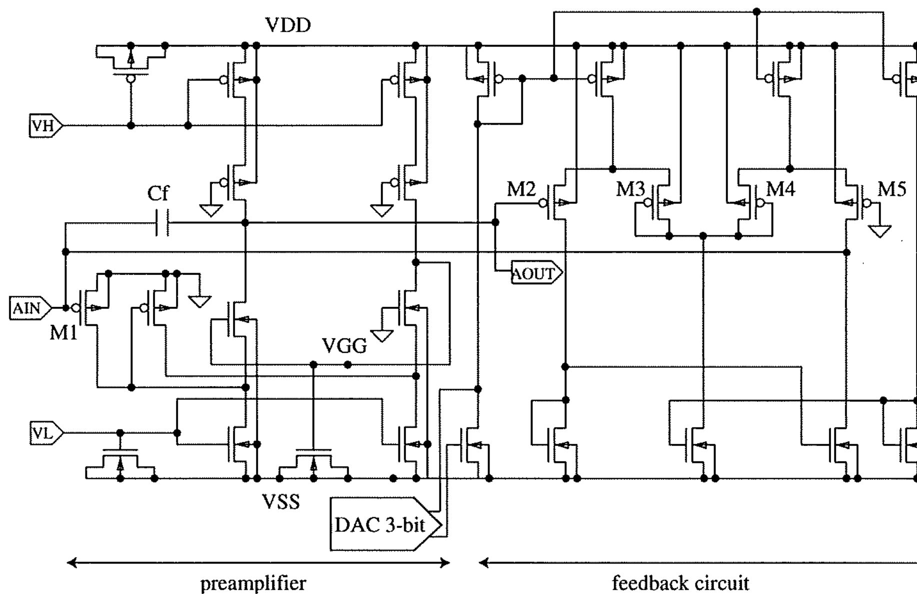

Fig. 3. Detailed schematic of the charge-sensitive amplifier.

Table 2
Parameters for the charge-sensitive amplifier

Main characteristics	PMOS input, gain-boost for cascode
Input transistor dimensions (W/L/M)	1440 μm/1.8 μm/180
Transconductance (g_m)	1.73 mS with $I_d = 107\,\mu$A
Effective impedance of feedback circuit (R_f)	$\simeq 400$ MΩ
Feedback capacitance (C_f)	0.02/0.04 pF

previous ASICs [9,10]. Feedback capacitor C_f can be selected among 0.02 and 0.04 pF.

2.4. High-resistance circuit

Fig. 4 shows a detailed schematic of the high-resistance circuit. Current I_R flows into a 20-kΩ resistor R according to the difference in voltage between nodes VIN and IOUT. Assuming matching among the geometrically identical MOS devices, I_R is divided between M1 and M2, or M3 and M4. The drain currents of M1 and M4 are given as $\frac{1}{5} \times I_R$, while those of M2 and M3 as $\frac{4}{5} \times I_R$. This partitioning factor is determined by the M value, which indicates the number of FET gates arranged in parallel. The following current mirrors of M5 to M6 and M7 to M8 set the output current at $\frac{1}{100} \times I_R$ at node IOUT. As a result, the overall circuit virtually boosts the impedance value of resistor R by an attenuation factor of 100, and thus functions as a 2-MΩ resistor. The reference current supplied from outside the chip is attenuated in the bias circuit and then applied to the high-resistance circuit as constant current sources (M9 and M10). Fig. 5 shows simulated frequency characteristics of the high-resistance circuit as obtained through circuit simulation. Eventually the effective impedances of R_2 and R_2' in Fig. 2 are about 1.5 MΩ (with an attenuation factor of 100), while those of R_1 and R_1' are about 6 MΩ (with an attenuation factor of 400).

2.5. Control scheme

Each channel contains a 15-bit configuration register. Three bits are used for switching the decay-time constant of the CSA, six bits for baseline equalization (three bits per filter circuit), three bits for threshold equalization, one bit for masking noisy channels, one bit for selecting the polarity of input signals, and one bit to enable the test input pulse. In addition, a five-bit central register is equipped to provide common settings among the channels. Two bits are used for selecting monitor output among the CSA and slow and fast filters, two bits for switching the peaking time of the filter circuits (one bit per filter circuit), and one bit for selecting the preamplifier gain ($C_f = 0.02$ or 0.04 pF). All bits are stores in D-type flip-flops.

3. Setup of performance measurements

In the experimental setup, the ASIC is held in a QFP-80 socket mounted on the test board. The test board is also placed in a light-shielded aluminum box. The interface with a computer is established using a National Instruments PCI-7833R board that contains a reconfigurable FPGA.

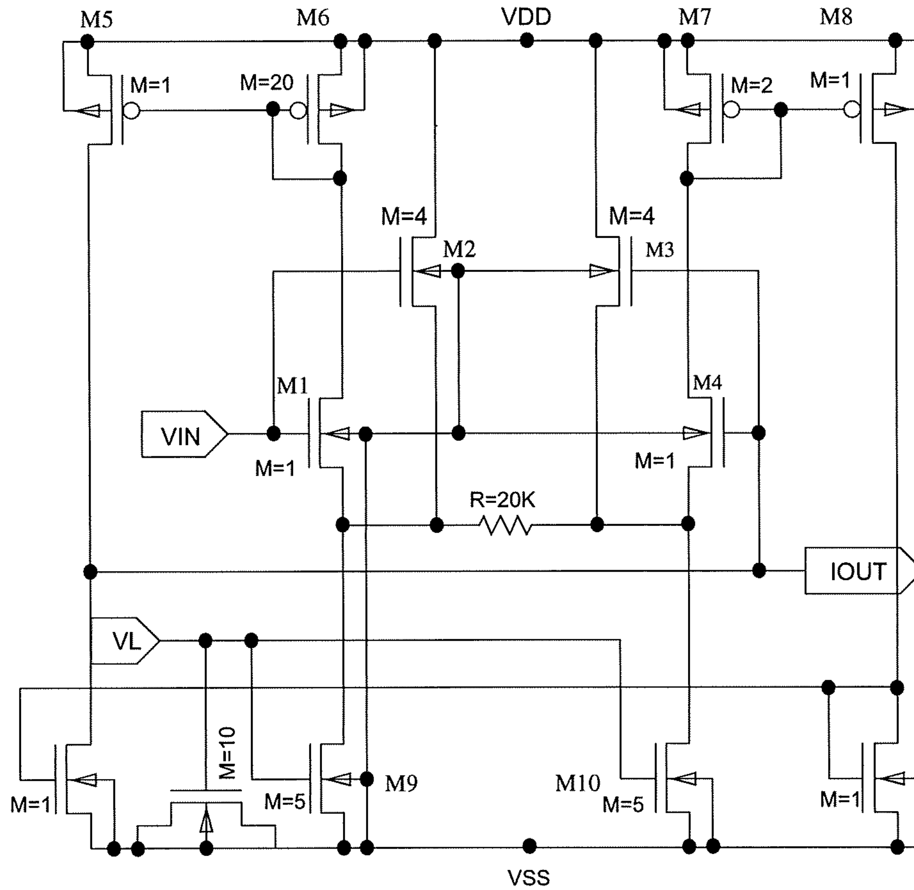

Fig. 4. Detailed schematic of the high-resistance circuit.

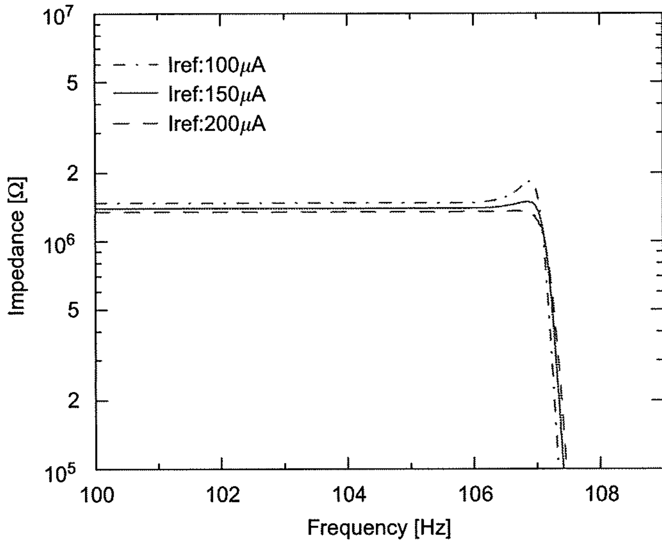

Fig. 5. Frequency characteristics of the high-resistance circuit with SPICE simulation. I_{ref} is a reference current supplied to a bias circuit connected to the resistance circuit.

LabView software tools were used to control the readout sequence. The interface signals are organized into three groups: CMOS inputs, LVDS inputs, and LVDS outputs. Since CMOS signals for the KW01 are operated with $V_{DD} = 1.65\,V$ and $V_{SS} = -1.65\,V$, the signals must be converted from or into LVTTL signals for the PCI-7833R board. Given the typical offset voltage of 1 V for commercial LVDS drivers, their outputs are leveled down in DC by 1 V before being fed into the chip. In order to mitigate interference with an analog processing chain, we chose LVDS for the trigger and hold signals.

4. Experimental results

4.1. Waveform of analog output

Fig. 6 shows the measured waveform traces of analog outputs with both positive and negative input charges of 2 fC. All measurements were performed in high gain mode (where $C_f = 0.02\,pF$). Although the peaking times are longer than in the simulation, the negative ones are closer to the design value. The pulse heights are consistent with the simulation results. As shown in the upper panel in Fig. 6, note that the undershoot or overshoot is not excessive even without a pole-zero-cancellation circuit. In the case of $T_M = 3\,\mu s$, $C_f R_f$ $(= 8\,\mu s)$ is not negligible compared with T_M and the undershoot is shown somewhat in the lower panel of Fig. 6. However, our application required no high count rate.

4.2. Linearity

Fig. 7 shows the linearity curves of a typical channel. The configuration settings are the same for both negative and positive input signals. As this figure shows, the linearity curves are consistent with the simulation results until a maximum output swing of about 1 V.

The lower panel of Fig. 7 shows the residuals between the measured data points and linear functions. Note that different linear functions are used for calculating the residuals between positive and negative polarities. The linearity curve between −4 and +3.5 fC is maintained with an integral nonlinearity of 5% in high gain mode ($C_f = 0.02\,pF$), while that between −10 and +7 fC in low gain mode ($C_f = 0.04\,pF$).

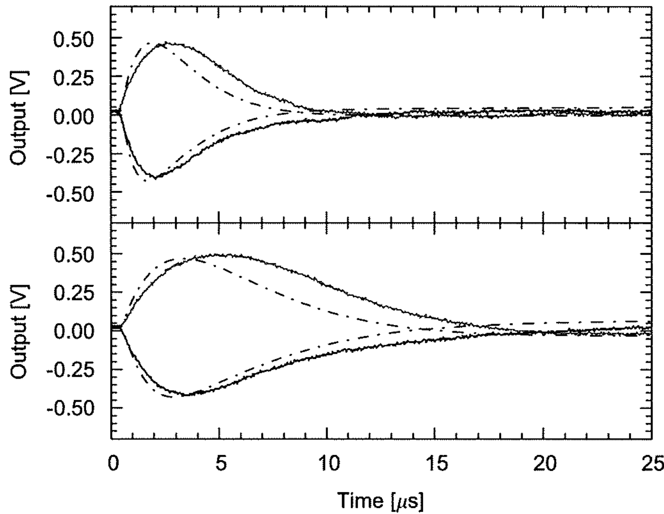

Fig. 6. Measured analog waveforms of a typical channel together with simulation data points (dot-dash line). The upper panel shows the data for $T_M = 1.5\,\mu s$ mode and the lower for $T_M = 3\,\mu s$ mode. The injected test pulse is 2 fC.

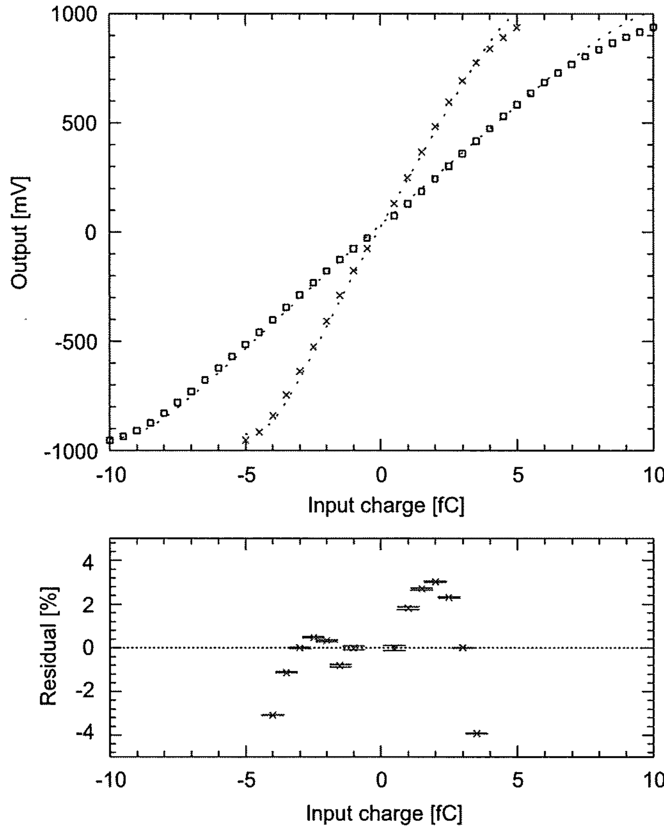

Fig. 7. Linearity curve of a typical channel. The measured data points are shown together with the simulation results (dotted line). The circles are the data points for $C_f = 0.04\,pF$ and squares for $C_f = 0.02\,pF$. The lower plots indicate the residuals between data points and linear functions.

4.3. Noise performance

Fig. 8 shows the measured noise performance. The rms noise is $188e^- + 7.5e^-/pF$ for a peaking time of 3 μs and $205e^- + 10.6e^-/pF$ for a peaking time of 1.5 μs. Although the noise slopes are nearly consistent with the simulation results, the curves have an excess of $210e^-$. The origin of that excess is being investigated. The measurements were performed with the ASIC in a plastic-mold package mounted on a burn-in socket, and thus the intrinsic noise level is expected to be lower than the measured value. The theoretically expected noise level is $48e^-$ at input capacitance of 0 pF.

4.4. Channel-to-channel variations in analog performance

The other aspects of analog performance were evaluated for 10 chips (a total of 80 channels). Table 3 summarizes the measurements.

Fig. 9 shows the distribution of the CSA baseline. We found that 11 channels strayed too far from ground level and did deliver analog outputs. This phenomenon is probably due to excessively large leakage current of the

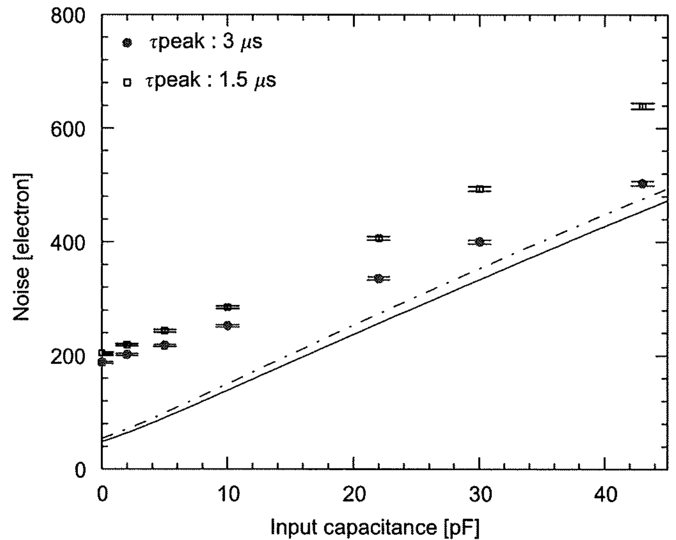

Fig. 8. Input capacitance versus noise level (ENC). The solid and dot-dash lines show results from a circuit simulation, and the circles and squares are the measured data points.

Table 3
Summary of analog performance

Gain	205 mV/fC for $C_f = 0.02$ pF, 112 mV/fC for $C_f = 0.04$ pF
Gain variation	5.5%
Noise level	$188e^- + 7.5e^-$/pF (rms)
Peaking time	3.93 or 1.95 μs
Peaking time variation (σ)	6.1% chip-to-chip

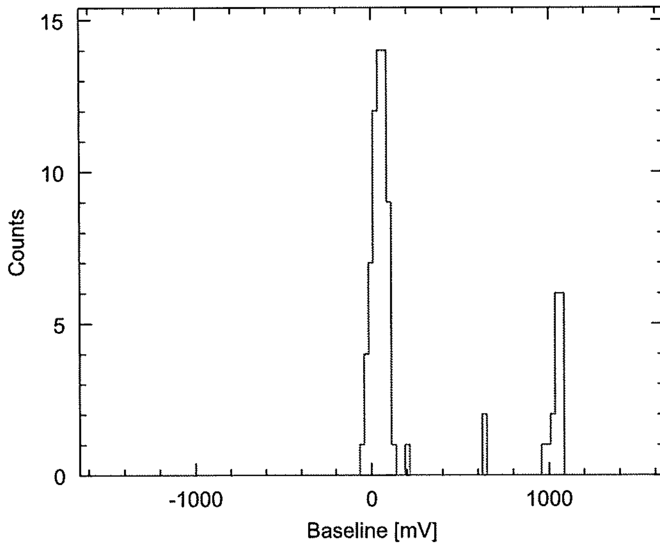

Fig. 9. Baseline distribution of the CSA.

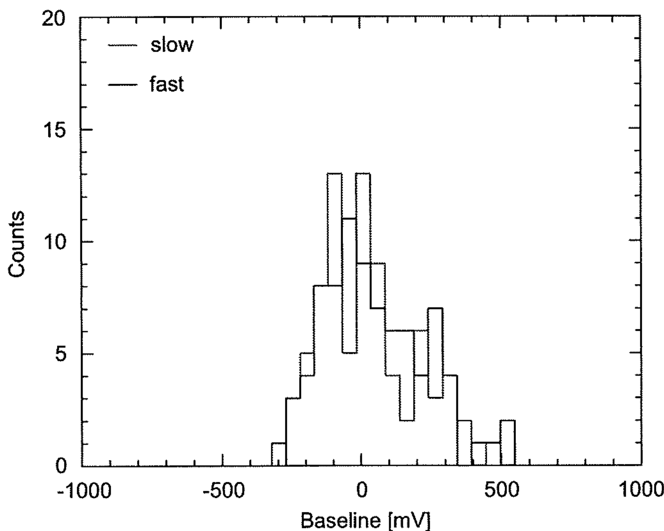

Fig. 10. Baseline distribution before adjustment.

ESD protection circuit in competing with the feedback current of the CSA. To resolve this problem, a leakage current compensation circuit will be employed in the next ASIC.

Figs. 10 and 11 show the baseline distribution before and after adjusting the offset DACs, respectively. The baseline distributions of the slow and fast filters without adjustment are 19 ± 169 and 6 ± 183 mV, respectively. Applying the

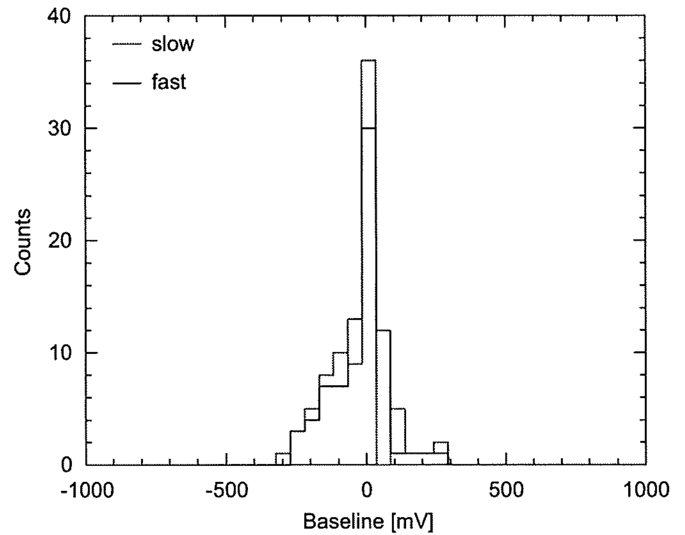

Fig. 11. Baseline distribution after adjustment.

baseline adjustment improves the distributions to -3 ± 60 and -2 ± 80 mV, respectively. However, these values are still larger than the trimming range of the threshold, which is 5 mV per bit. In the present ASIC, the baselines can only be adjusted in a negative direction, and thus the distribution is asymmetric and broadens in the negative direction. The baseline distribution may be due to the dispersion in components caused by irregularities in the manufacturing process. Therefore, the adjustable ranges of the offset DACs and trim DACs must also be extended for practical use.

5. Measurements with a CdTe detector

To verify low-noise performance, the ASIC must be assembled together with a CdTe detector. The detector is based on the high-quality single CdTe crystal manufactured by ACRORAD of Japan. With the use of indium (In) and platinum (Pt) for the anode electrode and cathode electrode, respectively, this device works as a Schottky diode. This device has lower leakage current than ohmic detectors and allows higher bias voltages to be applied, leading to almost full charge collection [20]. Moreover, the cathode electrode is covered by a guard ring to reduce the leakage current of the detector [21]. The detector measures 2.4 × 2.4 mm in size and 0.5-mm thick, and is covered by a guard ring 1 mm in width.

Since the spectral performance depends on the leakage current and detector capacitance, the leakage current must be measured before connection with the ASIC. Positive voltages were applied to the indium electrode using a Keithley 237, and current on the cathode side was measured using a Keithley 6517A. As a result, the measured leakage current was 12 pA with a bias voltage of 600 V at 20 °C, and the detector capacitance was 1.2 pF.

Fig. 12 shows the setup for the spectral measurements. An electric wire of about 1 cm is used for connection

between the active area of the cathode electrode and the DIP socket mounted on the test board. The DIP socket is wired to the QFP-80 socket pins corresponding to the CSA input. We obtained the gamma-ray spectra of radioactive sources ^{241}Am (in Fig.13) and ^{57}Co (in Fig. 14) with $C_f = 0.02$ pF and self-trigger mode at an operating temperature of 20 °C and a bias voltage of 600 V. The channel peaking time was measured using the waveform before obtaining the spectra, and its value was 4.13 μs with the detector. The energy resolution is 2.51 keV (FWHM) for a gamma ray of 59.5 and 2.35 keV (FWHM) for a gamma ray of 122 keV. The test pulse spectra were obtained with an injected charge of 2 fC (equivalent to about 55.4 keV in the CdTe detector) and shifted in right direction for comparison. As for the ^{57}Co spectrum, the gain was carefully calibrated with a quadratic function, because the peak energy of 122 keV is around the maximum output swing of 1 V. Note here that common mode noise correction was not performed for the output amplitude of the ASIC.

According to the width of pedestal distribution, the observed noise is 259e$^-$ (rms), while the noise level of this channel without the detector is 212e$^-$ (rms). Thus, the noise residual is given as 149e$^-$(= $\sqrt{(259)^2 - (212)^2}$). The contribution of the equivalent noise charge (Q_n^2) from the leakage current (I_d) is calculated by the first term of Eq. (7) as follows:

$$Q_n^2 = 12 \cdot \left[\frac{e^2}{nA \cdot ns}\right] \cdot I_d \cdot T_M \quad (8)$$

where the equivalent noise charge is expressed in electrons. If we assume $T_M = 3.93$ μs and $I_d = 12$ pA, the noise contribution from the detector leakage current is 24e$^-$. This value is too small to explain the noise residual. The origin of the excess noise is being investigated, although we speculated that the parasitic capacitance, which may be caused by an assembly issue, is added to the total input capacitance. To address this assembly issue, we are now designing a low-noise ceramic carrier for the bare chip.

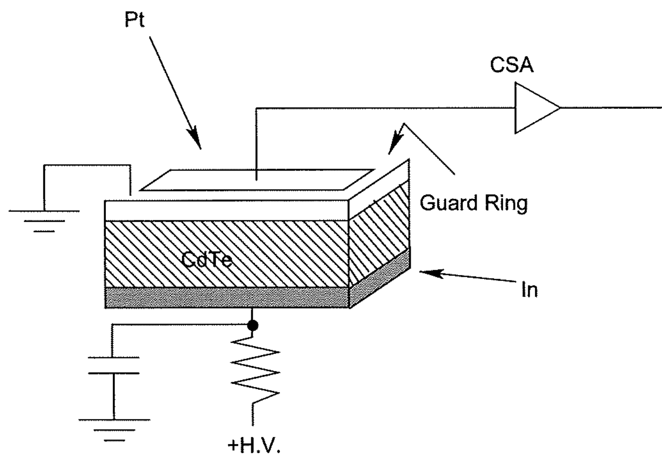

Fig. 12. Setup of the spectral measurements with a CdTe diode detector. The cathode face (Pt) is divided into the guard ring and the central plane (active area).

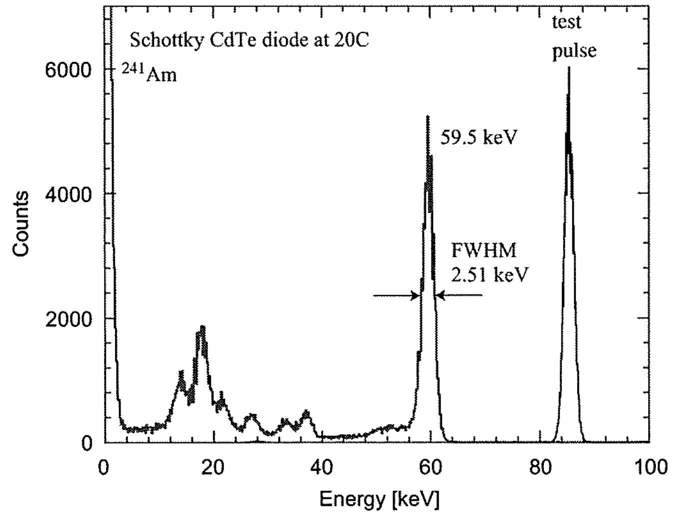

Fig. 13. Spectrum of ^{241}Am with the ASIC connected to a Shottky CdTe diode. The CdTe measures 2.4 × 2.4 × 0.5 mm in size and has a guard ring. The bias voltage is 600 V and operating temperature 20 °C.

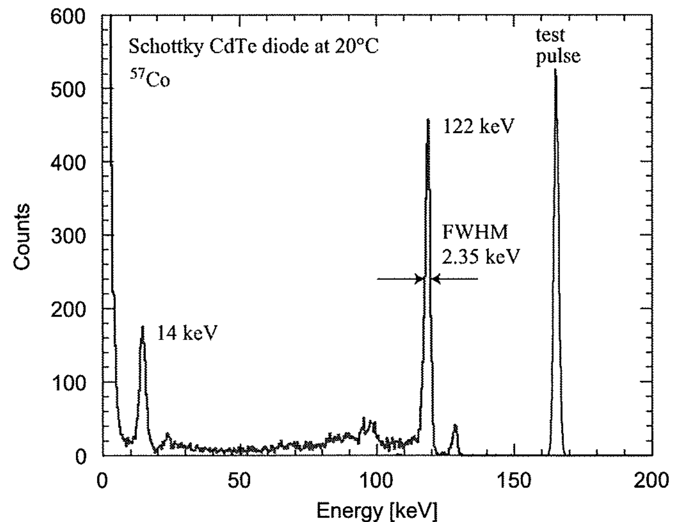

Fig. 14. Spectrum of ^{57}Co with the ASIC connected to a Shottky CdTe diode. This is obtained in the same condition as the spectrum of ^{241}Am.

6. Conclusion

We are developing low-noise front-end ASICs to read out CdTe detectors for future astrophysical applications. In order to establish low-noise circuit architectures, an eight-channel ASIC has been developed based on the Open-IP LSI project. By using the newly designed high-resistance circuit, the ASIC operates both for positive and negative signals with a wide dynamic range up to an input charge of 7 fC. The equivalent noise level of 188e$^-$ + 7.5e$^-$/pF (rms) has been reached for power consumption of 4 mW per channel. To verify the low-noise characteristics, we combined the ASIC with a CdTe diode detector

and obtained the gamma-ray spectra of radioactive sources. The energy resolutions were 2.51 keV (FWHM) for a gamma ray of 59.5 and 2.35 keV (FWHM) for a gamma ray of 122 keV at room temperature. We are now designing a low-noise ceramic carrier to be assembled with the bare chip. In addition, a robust version of the ASIC including a leakage current compensation circuit is also being developed.

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NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

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Development of double-sided silicon strip detectors (DSSD) for a Compton telescope

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Abstract

The low noise double-sided silicon strip detector (DSSD) technology is used to construct a next generation Compton telescope which is required to have both high-energy resolution and high-Compton reconstruction efficiency. In this paper, we present the result of a newly designed stacked DSSD module with high-energy resolution in highly packed mechanical structure. The system is designed to obtain good P-side and N-side noise performance by means of DC-coupled read-out. Since there are no decoupling capacitors in front-end electronics before the read-out ASICs, a high density stacked module with a pitch of 2 mm can be constructed. By using a prototype with four-layer of DSSDs with an area of 2.56 cm × 2.56 cm, we have succeeded to operate the system. The energy resolution at 59.5 keV is measured to be 1.6 keV (FWHM) for the P-side and 2.8 keV (FWHM) for the N-side, respectively. In addition to the DSSD used in the prototype, a 4 cm wide DSSD with a thickness of 300 μm is also developed. With this device, an energy resolution of 1.5 keV (FWHM) was obtained. A method to model the detector energy response to properly handle split events is also discussed.
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Keywords: Silicon strip detector; Compton telescope; Gamma-ray astronomy

1. Introduction

The observation of high-energy astrophysical phenomenon utilizing sub-MeV/MeV gamma rays is an attractive result that opens up a new window for studying particle acceleration and nucleon synthesis in the universe. However, the sensitivity is limited because of high background, low efficiency, and the difficulty of imaging utilizing focussing technology. As demonstrated by COMPTEL [1] onboard CGRO (Compton Gamma-Ray Observatory), in the range from ~1 to several tens of MeV, a significant reduction of background by means of reconstructing Compton scattering is proved to be useful in this difficult spectral band.

Our approach is to apply the concept of Compton telescope in the range of several 10 keV to several 100 keV. In order to extend the capability down to low energy gamma rays, the use of a stack of double-sided silicon strip detectors (DSSD) [2] is very attractive. Taking advantage of significant progress in technology related to Si and CdTe imaging detecors, we are developing a new generation of Compton telescope, the semiconductor Compton telescope (Si/CdTe Compton telescope) [3–8]. Si works as a good scattering medium because the cross-section of Compton scattering becomes larger than that of photo-absorption above 50 keV. In addition, the advantage of Si is its

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relatively small Doppler broadening effect [9] compared with Ge or CdTe [10]. On the other hand, CdTe works very nicely as an absorber thanks to its high atomic number and high density.

The scattering part is very important in the Compton telescope. In order to cover an energy range from several 10 keV, the energy threshold of the detector must be low, because the energy of recoil electrons is almost below 10 keV in this energy band. Furthermore, a high Compton scattering probability is desirable to obtain a high efficiency as a Compton telescope. In the Si/CdTe Compton telescope, we employ a DSSD module that consists of compactly stacked layers of DSSDs (Fig. 1). In order to be hermetically and symmetrically enclosed by absorbers, the scattering part needs to have a compact structure. Also, a symmetrical structure is desirable to reduce possible systematic errors in measurements of linear polarization of gamma rays.

In order to demonstrate the concept of the Si/CdTe Compton telescope, we have developed high-quality DSSD together with a low noise analog ASIC to realize a noise level as low as 1–2 keV (FWHM) [11,12]. As a next step, we work on improving the Compton scattering efficiency. The development of a large volume and high-density DSSD module is a key to achieve the requirements. In addition, the mass of the supporting materials including the read-out electronics should be minimized to reduce the interaction of scattered photons with inactive materials. The improvement of the N-side energy resolution also increases the efficiency. In a previous prototype, an energy resolution of 1.3 keV (FWHM) on the P-side is achieved, while 3.8 keV on the N-side. Thus, an improved N-side resolution makes it possible to determine the position of Compton scattering with high accuracy for smaller energy deposits.

In this paper, we present the results of the new prototype of stacked DSSD module which emphasizes energy resolution and density in Section 2. Next, the results from a 4 cm wide DSSD which improves the Compton scattering efficiency is reported in Section 3. Finally, a detailed DSSD energy response including inter-strip events is discussed in Section 4.

2. Prototype of high density stacked DSSD module

2.1. The new DSSD board

The DSSD used here is the 2.56 cm wide device developed with Hamamatsu Photonics, Japan. See Tajima et al. [12] for the details of this device. The device was produced from an n-type wafer which has resistivity of 5 kΩ cm. The wafer thickness is 300 μm. The N-side has a floating p-implantation between strips to isolate adjacent strips. The strip pitch is 400 μm and the width is 300 μm on each side. The Al electrodes are DC-coupled on each implantation.

A photograph of the newly developed DSSD board is shown in Fig. 2. It consists of one DSSD and two specially designed low noise analog VLSI, VA64TAs, mounted on a small circuit board. The VA64TA is manufactured by IDEAS ASA, Norway in collaboration with us. It has a 64 channel input and can be used for both positive and negative input charges. Combined with the compact design, the support structure is made of plastic instead of Al_2O_3 ceramic. The average thickness of the support in the horizontal direction is 1.4 g/cm^2.

A DC-coupled read-out is employed not only on the P-side but also on the N-side to obtain good energy resolution. To apply reverse voltage, the N-side circuit as a whole is biased by 100 V. The decoupling is performed in the read-out system as described later. Since this system does not need decoupling capacitors in front-end, it becomes possible to shorten the stack pitch to 2 mm from 6 mm in a previous prototype [5,6].

2.2. Four-layer stacked DSSD module

Combining the new DSSD board, a four-layer stack of the DSSD module is constructed. Fig. 3 shows the

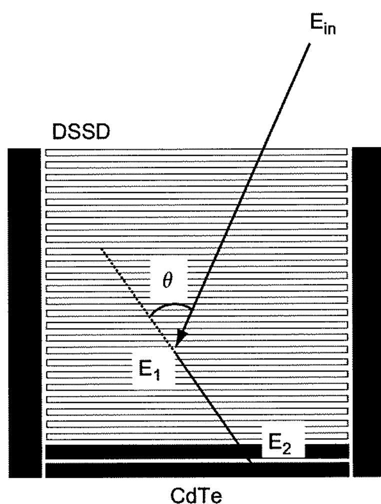

Fig. 1. Design of stacked DSSD module with CdTe detectors (absorbers).

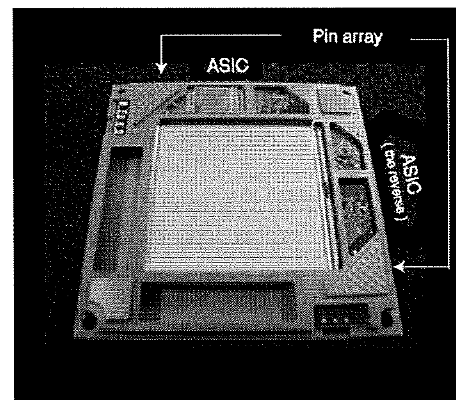

Fig. 2. Photograph of a DSSD board.

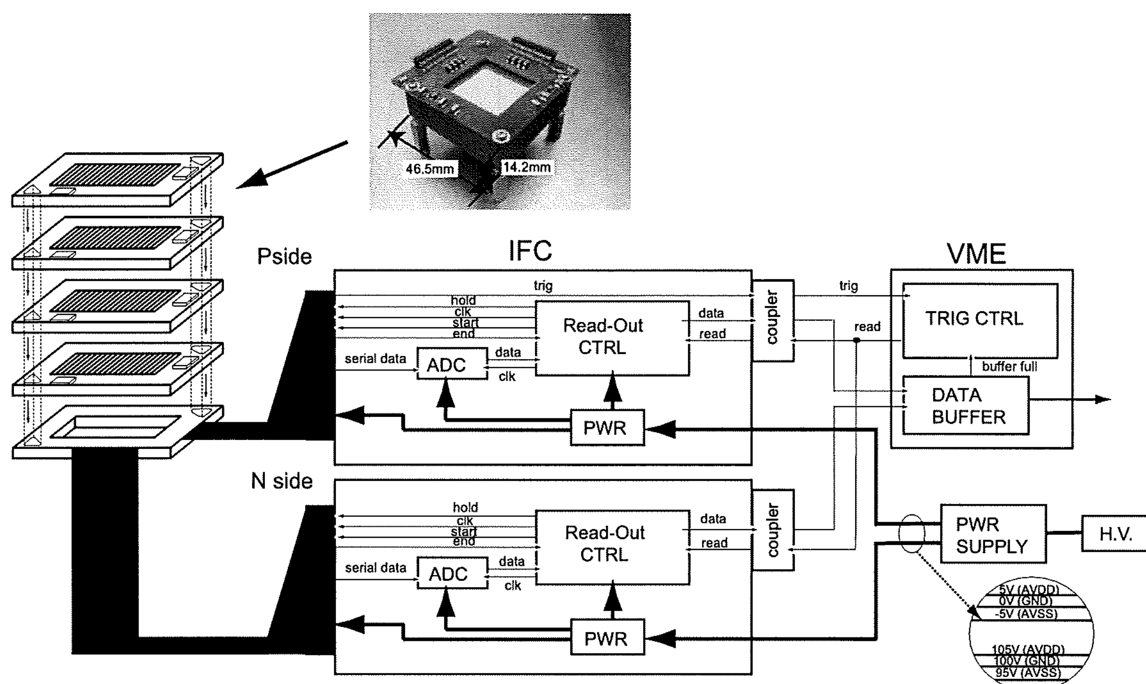

Fig. 3. Schematic diagram of the four-layer stacked DSSD module.

schematic diagram of the system. Four DSSD boards are daisy-chained via pin arrays and stacked with a 2 mm pitch. Each side has the same read-out board, the Inter Face Card (IFC), which controls the read-out sequence. The IFC interchanges the digital signal with the external system via an ultra fast coupler with 2000 V tolerance, hence we can supply the reverse bias to each DSSD by means of operating two IFCs under voltage gap corresponding to reverse bias. Consequently, we can realize DC-coupled read-out on both sides.

All layers were successfully operated at −20 °C and a bias of 100 V. In Fig. 4, we present sum spectra of both the P-side and N-side in each layer. The energy resolution at 59.5 keV is obtained to be 1.6 keV (FWHM) in P-side, which is about 0.3 keV larger than the expected value calculated from VA64TA noise performance and the input capacitance of DSSD. The difference is explained by the pitch adapter capacitance between the DSSD and LSI since we observed 1.2 keV (FWHM) for the channels with a short pitch adapter. We are currently fabricating a new LSI with optimized input channel pitch to minimize the length of the pitch adaptor.

In spite of the effect of the pitch adapter capacitance, we recognize an improvement of the N-side energy resolution from 3.8 to 2.8 keV (Fig. 4 right), compared with AC-coupled read-out with RC-bias chip [11] with $R \simeq 4\,\mathrm{G\Omega}$ and $C \simeq 50\,\mathrm{pF}$ in the previous prototype [5,6]. The noise on the N-side is still larger than what was expected from the LSI performance and the total capacitance load. The origin of this "excess noise" is under investigation.

3. A 4 cm wide DSSD

Another way to increase the efficiency is to enlarge the DSSD itself. We have developed a 4 cm wide DSSD for the future stacked DSSD module. Although the preliminary results are already summarized by Nakazawa et al. [13], we here present the detailed performance of the device including energy response. The strip length is 3.84 cm and thus the effective area (active area × thickness) is 2.25 times larger than the 2.56 cm wide DSSD. The strip parameters are the same to these of the 2.56 cm wide DSSD. The thickness is 300 μm, while the strip pitch is 400 μm and the width is 300 μm on both sides.

3.1. Basic characteristics of the device

We measured the leakage current of two selected strips in the P-side using a KEITHLEY 237 multimeter. The I–V curve of the 4 cm DSSD with various temperatures and bias voltages is presented Fig. 5 (left). The leakage current at 100 V bias is 650 pA at 20 °C and 26 pA at −10 °C. These values are about 1.6 times larger than a 2.56 cm wide DSSD, proportional to the size of the device.

A DSSD capacitance has two origins: the body capacitance and the inter strip capacitance. We measured these capacitances using a HP4284A multimeter. The result is shown in Fig. 5 (right). The body capacitance per strip becomes constant at a value of 5 pF above a bias of 70 V. This means that the full depletion voltage is 70 V. However, the N-side inter strip capacitance still decreases even above 70 V and becomes constant around 100 V. This fact

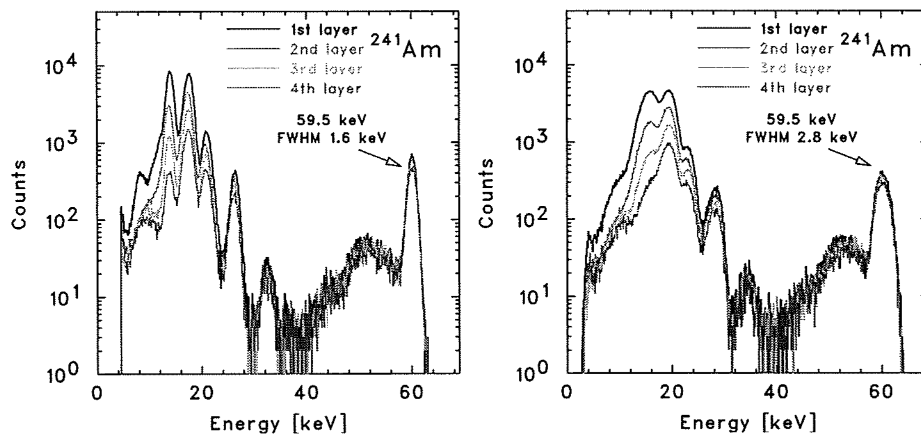

Fig. 4. Sum spectra for each layer (left: P-side, right: N-side).

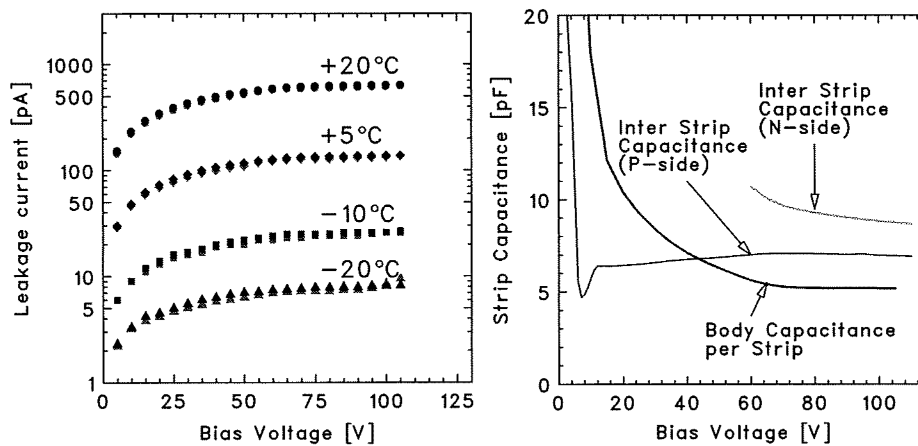

Fig. 5. Measured basic property of 4 cm wide DSSD. *I–V* curve with various temperature (left), *C–V* curve (right).

suggests that actually a 100 V bias is required to make the N-side inter strip fully isolated. Since total input capacitance is a sum of the body capacitance and the inter strip capacitance, we can estimate it as 12.2 and 14.2 pF at the P-side and N-side, respectively.

3.2. Imaging and spectroscopy

We read out the 4 cm wide DSSD using another analog LSI, VA32TA [12]. The 4 cm wide DSSD has a total of 192 channels, so we need 6 VA32TA chips. In this experiment, we apply reverse bias via a RC-bias chip on the N-side.

The DSSD was operated at −10 °C with a 100 V bias. The left panel of Fig. 6 is ^{133}Ba line image integrated in the energy band from 20 to 40 keV. The classic style car mask, made of 0.3 mm thick brass, was mounted 3 mm above the DSSD. The right panel of Fig. 6 is the sum spectra of all 96 strips in the P-side. The energy resolution at 59.5 keV is measured to be 1.5 keV (FWHM). This energy resolution is consistent with the value which is calculated from the VA32TA noise performance and input capacitance.

3.3. Pulse height correlation

We irradiated two adjacent P-side strips (Nos. 73 and 74) with 59.5 keV gamma rays from ^{241}Am. Since the attenuation length is 1.34 cm [14] for 60 keV photons, interactions occur almost uniformly in the 300 μm thickness. Fig. 7 is the distribution of the pulse height correlation. The regions surrounded by rectangles with oblique lines are lower energy lines of ^{241}Am. The distribution shows that our DSSD has roughly 10% split events which share signals between adjacent strips.

The striking feature of the plot is the opposite polarity events which are of unknown origin. This phenomenon is not detected in the same diagram generated for N-side. Because of the threshold of our measurement, we can predict that some events are undetected even though they actually interact in the DSSD. Thus there are "dead events" in the DSSD. The phenomenon is not only observed in a 4 cm wide DSSD but also in a 2.56 cm wide DSSD. The 4 cm DSSD has statistical advantage because of its larger effective area, thus it is suitable for a detailed investigation of energy response.

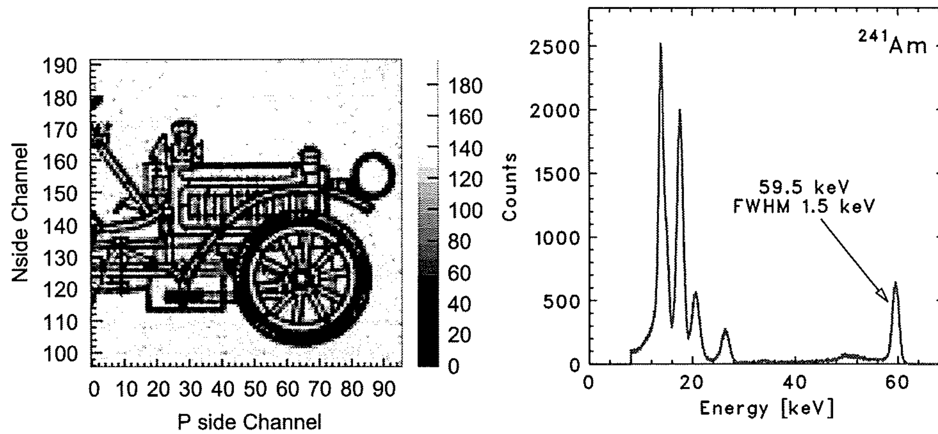

Fig. 6. A shadow image ranging from 20 to 40 keV X-ray irradiated ^{133}Ba (left), a sum spectrum of P-side irradiated ^{241}Am (right).

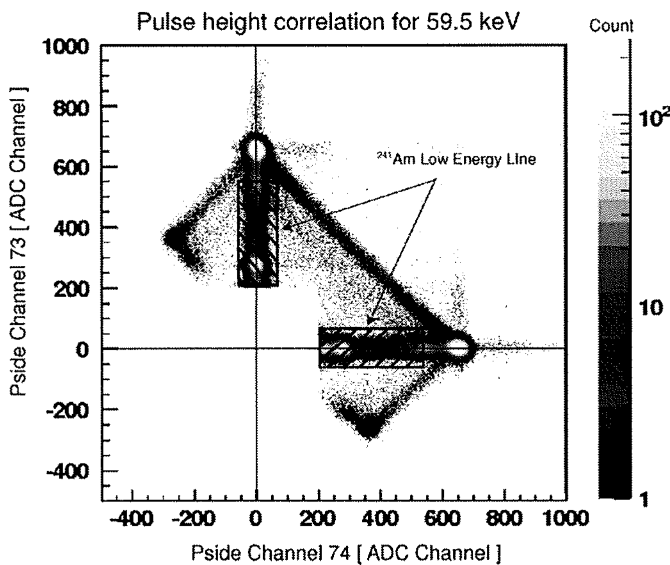

Fig. 7. Pulse height correlation between strip Nos. 73 and 74.

Since the effect will not be negligible in Compton reconstruction, we should identify the origin of these events and evaluate the percentage of the "dead events". In the next section, we discuss these phenomenon, based on two-dimensional device simulator and the assumption of a simple charge induced model.

4. Detailed energy response of DSSD

4.1. Potential simulation

As the first step, the internal potential of the DSSD was calculated using the two-dimensional device simulator VENUS-2D, developed by Fuji Research Institute Corporation, Japan. The geometry is a cross-section perpendicular to the p-strip. We estimate the donor density of n-bulk silicon as $8.3 \times 10^{11}\,cm^{-3}$ from our DSSD's resistivity and set p^+ and n^+ dope density as a typical value $1.0 \times 10^{18}\,cm^{-3}$. Additionally, we set the positive fixed oxide surface charges

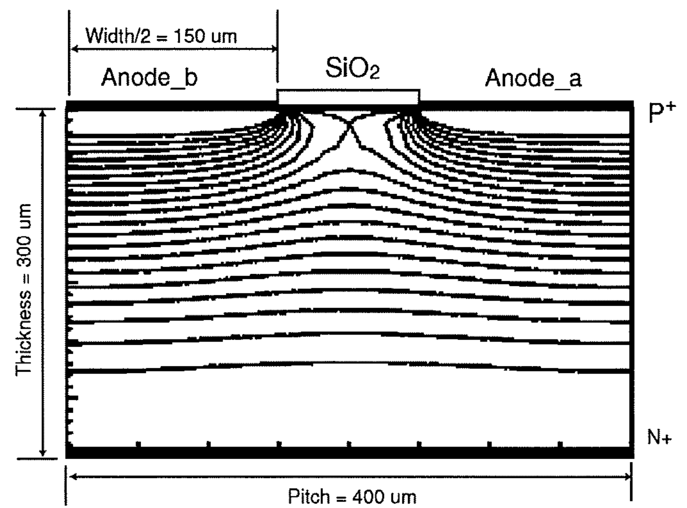

Fig. 8. Internal potential of DSSD under full depletion voltage.

in the Si–SiO_2 transition region to have a typical value $1.0 \times 10^{12}\,e/cm^2$ [15]. This geometry fully depletes on bias voltage around 60 V, the value of which is consistent with the actual measurements (Section 3.1).

Fig. 8 is a simulated internal potential under full depletion voltage. Positive fixed oxide surface charges induce local minimum potential between the p-strips and in this region electrons are conducted to the center of SiO_2 layer, not to N-side. The local minimum potential region extends to about $1500\,\mu m^2$ under SiO_2 layer.

4.2. Simulated pulse height correlation

Based on the potential simulation, we next calculated the pulse height correlation between the two anodes (Anode_a and Anode_b in Fig. 8) for 59.5 keV photo-absorption events. To estimate the charge collection, we introduce simple assumptions as follows:

(1) Holes and electrons are fully conducted either to electrodes or to the SiO_2 layers.

(2) The trajectory of a charge is simply defined by the potential taking no account of initial momentum and thermal diffusion.
(3) Electrons ($-Q$) conducted to SiO_2 induce the same amount of signal ($+\frac{1}{2}Q$) to the adjacent strips (Anode_a, Anode_b) (see Yorkston et al. [16] for experimental evidence).
(4) The initial charge cloud size is defined as $C_{\text{init}} \simeq 0.0171 \times T_e^{1.75}$ (μm) [17], where, C_{init} is the 2 sigma cloud diameter and T_e is the initial electron kinetic energy. For example, $C_{\text{init}} = 21$ μm for 59.5 keV photon absorption.

Fig. 9 is the result of the simulated pulse height correlation. The distribution (Fig. 9 top) is like an oblique rectangle which has the apex $(q, 0)$, $(\frac{1}{2}q, -\frac{1}{2}q)$, $(-\frac{1}{2}q, \frac{1}{2}q)$, $(0, q)$. This corresponds to the experiment (Section 3.3). The reason of forming this distribution is because the amount of charge collection to Anode_a and Anode_b varies according to the point where the initial cloud is generated. We can roughly divide the internal region into eight sections as indicated in Fig. 9 bottom, A–G. All holes move to the nearest strip and all electrons move to N-side in A $(q, 0)$ and G $(0, q)$. All holes move to the nearest strip and electrons are shared between SiO_2 and N-side in B (between $(q, 0)$ and $(\frac{1}{2}q, -\frac{1}{2}q)$) and F (between $(-\frac{1}{2}q, \frac{1}{2}q)$ and $(0, q)$). All holes move to the nearest strip and all electrons move to SiO_2 in C $(\frac{1}{2}q, -\frac{1}{2}q)$ and E $(-\frac{1}{2}q, \frac{1}{2}q)$. Holes are shared between strips and all electrons move to SiO_2 in D (between $(\frac{1}{2}q, -\frac{1}{2}q)$ and $(-\frac{1}{2}q, \frac{1}{2}q)$). Holes are shared between strips and all electrons move to N-side in H (between $(0, q)$ and $(q, 0)$).

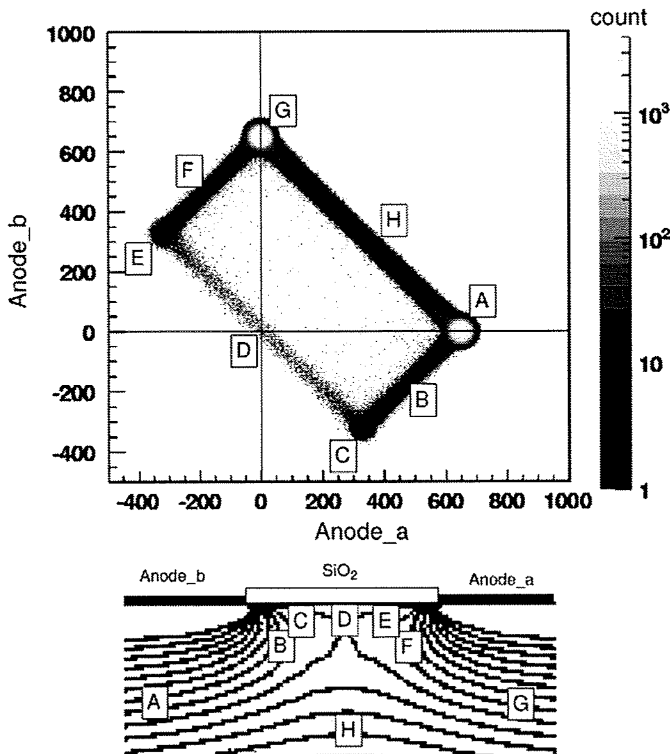

Fig. 9. Simulated pulse height correlation between adjacent strips. According to the region where initial cloud is generated, the distribution becomes oblique rectangle.

Table 1
Comparison between actual experimental data (Fig. 7) and simulation results (Fig. 9)

Region	Number of events (normalized)	
	Experiment	Simulation
A+G	100	100
H	6.3	4.1
(B+C)+(E+F)	4.5	2.0
D	N/A	0.08

Regions A to H are indicated in Fig. 9. Number of events are normalized to those in the A+G region, which is set to 100.

Table 1 shows a comparison of event distributions between experiment (Fig. 7) and simulations (Fig. 9, top). Simulations reproduce the experimental data well. In Section 3.3, we reported on the presence of "dead events". They are shown to originated from the region D (Fig. 9, bottom). In experimental data (Fig. 7), the density of these events is slightly higher than those of the simulation. This is well explained as a contribution of gamma rays below 59.5 keV, such as backscatter events around 48.3 keV (Fig. 7). Although the threshold of measurement and mixed response for different energy photons in the diagram of pulse height correlation make it difficult to measure the probability of "dead events", we predict from simulation that their probability is on the order of 0.1%.

5. Summary and future prospects

Successful operation of the four-layer stack of a DSSD module with a stack pitch of 2 mm is demonstrated. The DC-coupled read-out is employed on both the P-side and the N-side. The energy resolution of 1.6 keV (FWHM) on P-side and 2.8 keV on N-side is measured for 59.5 keV X-ray at a temperature of −20 °C. The satisfactory performance of the 4 cm wide DSSD which has 2.25 times larger effective area than a 2.56 cm wide DSSD is also demonstrated.

The presence of "dead events" is found from the diagram of pulse height correlation for 59.5 keV incident photons. A two-dimensional device simulation with simple assumptions on charge collection can reproduce the energy response observed in the data well. We conclude from the simulation that the fraction of "dead events" is on the order of 0.1%, originating from the region of the local potential minimum under the SiO_2 layer.

Further approaches for a next revision of the stacked DSSD module include a new circuit board with shorter pitch adapter and an ASIC with an optimized input pitch and on-chip digitizer. As for the detector development, tests of DSSDs with a thickness of 500 μm and size of 4 and 2.56 cm are under progress. We also plan to fabricate a 5.12 cm^2 DSSD with a thickness of 500 μm to achieve 2.5 times larger effective area than a 4 cm wide DSSD

with a thickness of 300 μm without increasing the strip capacitance.

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NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

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Development of semiconductor imaging detectors for a Si/CdTe Compton camera

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Abstract

Si and CdTe semiconductor imaging detectors have been developed for use in a Si/CdTe Compton camera. Based on a previous study using the first prototype of a Si/CdTe Compton camera, new detector modules have been designed to upgrade the performance of the Compton camera. As the scatter detector of the Compton camera, a stack of double-sided Si strip detector (DSSD) modules, which has four layers with a stack pitch of 2 mm, was constructed. By using the stack DSSDs, an energy resolution of 1.5 keV (FWHM) was achieved. For the absorber detector, the CdTe pixel detector modules were built and a CdTe pixel detector stack using these modules was also constructed. A high energy resolution ($\Delta E/E \sim 1\%$) was achieved. The improvement of the detection efficiency by stacking the modules has been confirmed by tests of the CdTe stack. Additionally, a large area CdTe imager is introduced as one application of the CdTe pixel detector module.
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1. Introduction

The Compton camera is the most promising approach for gamma-ray imaging and spectroscopy in the range of several tens keV to several MeV. For Compton cameras, both good energy resolution and good position resolution are very important to achieve a Compton reconstruction that has high levels of accuracy. We propose a new concept of the Si/CdTe semiconductor Compton cameras based on our developments of Si and CdTe semiconductor imaging detectors [1,2].

The basic concept of the Si/CdTe Compton camera is shown in Fig. 1. Double-sided Si strip detectors (DSSDs) are used as scatterers and CdTe pixel detectors are used as absorbers. In order to increase the efficiency of Compton scattering, the DSSDs are tightly stacked in many layers. The CdTe pixel detectors are arranged around the DSSD stack to detect scattered gamma-rays with high efficiency.

When a gamma-ray photon is scattered in one DSSD and absorbed in one CdTe pixel detector, the incident energy of the gamma-ray and the scattering angle can be determined as

$$E_{\text{in}} = E_1 + E_2 \quad (1)$$

$$\cos\theta = 1 - \frac{m_e c^2}{E_2} + \frac{m_e c^2}{E_1 + E_2} \quad (2)$$

where E_{in} is the incident energy, E_1 is the energy of the recoil electron detected in the DSSD, E_2 is the energy of the

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scattered photon absorbed by the CdTe and θ is the scattering angle. If one measures the Compton scattering point, recoil electron energy, and scattered gamma-ray energy and position relative to the Compton scattering point, then the energy of the incident gamma-ray is determined, and the direction of the incident gamma-ray lies somewhere on a cone defined by these measurements.

The combination of Si and CdTe is suitable for gamma-rays that range from several tens of keV to a few MeV. The photo-absorption cross-section of Si is small, and the Compton cross-section becomes relatively large because of the small atomic number of Si ($Z = 14$). Additionally, Si works better than other materials with larger atomic numbers in terms of the "Doppler broadening" effect [3].

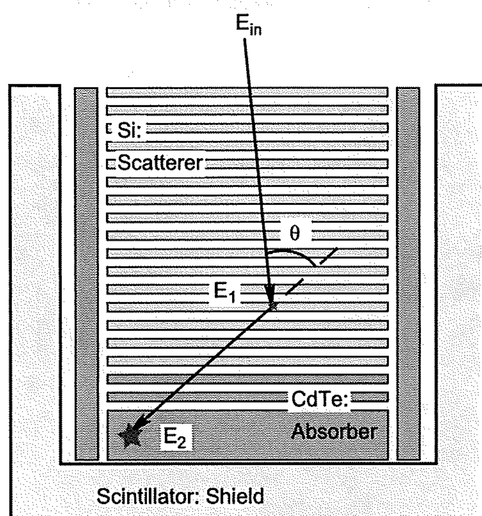


Fig. 1. Schematic picture of our Si/CdTe semiconductor Compton camera.

On the other hand, CdTe has high photo-absorption efficiency for gamma-rays in this energy region, due to their high atomic numbers of 48 and 52.

2. The results from the first prototype of the Si/CdTe Compton camera

We constructed a prototype of the Si/CdTe Compton camera in order to demonstrate the concept described above [4,5]. The prototype consisted of six layers of DSSDs and three CdTe pixel detectors. The DSSD has an area of 2.56 cm × 2.56 cm and a thickness of 300 μm. The strip pitch of the DSSD is 400 μm and each side has 64 strips. The CdTe pixel detector is based on the Schottky CdTe diode device, utilizing indium as the anode and platinum as the cathode [6,7]. The CdTe crystal is manufactured by ACRORAD in Japan using the Traveling Heater Method. The detector has dimensions of 18.55 mm × 18.55 mm and a thickness of 500 μm. The indium side is used as a common electrode. The platinum side is divided into 8 × 8 pixel sections surrounded by a 1 mm wide guard ring. The pixel size is 2 mm × 2 mm, and the gap between the pixels is 50 μm. Each pixel is connected to a fanout board by using In/Au stud bump bonding technology [8]. The signals from the DSSDs and CdTe pixel detectors are processed by low noise analog ASICs, VA32TAs.

By irradiating the prototype with gamma-rays from radio isotopes (^{133}Ba, ^{57}Co, ^{22}Na and ^{137}Cs), we have successfully obtained Compton reconstructed images and spectra from 80 to 662 keV. Fig. 2 shows Compton reconstructed images of ^{133}Ba and ^{22}Na sources obtained with the Compton camera. These images are drawn using conventional Compton reconstruction. First, we select "two-hit events"; that is, one hit to the DSSD and one

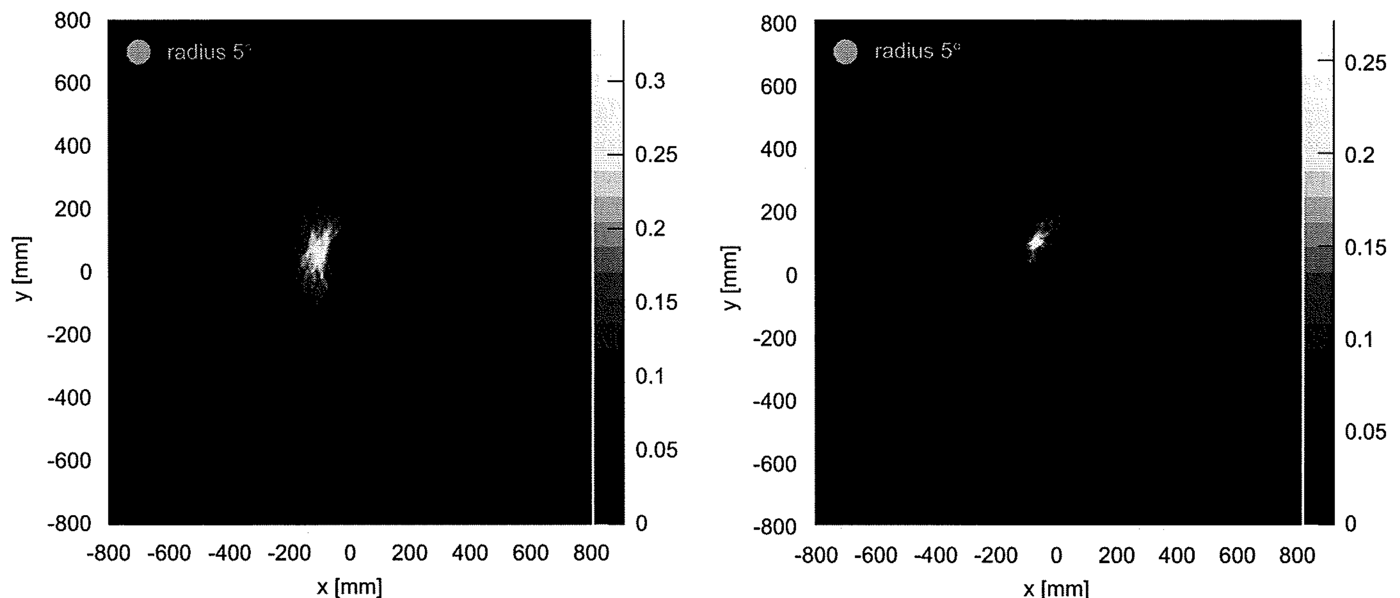


Fig. 2. Compton reconstructed images of 80 keV gamma-rays from ^{133}Ba (left) and 511 keV gamma-rays from ^{22}Na (right). Circles with a radius of 5° are drawn together with the images.

hit to the CdTe. The scatter angle is obtained for each two-hit event. From the scatter angle and the two-hit positions, a Compton cone is drawn on the sky event by event. We then project the cone onto the plane, and obtain the final image.

Due to the good energy resolution of both the DSSDs and the CdTe pixel detectors, good angular resolution was obtained. The achieved angular resolution almost reaches the theoretical limit due to Doppler broadening. Additionally, an important point to note is that the Compton reconstruction for low energy gamma-rays such as 80 keV is achieved. When 80 keV gamma-rays are scattered, the energy of the Compton recoiled electron is only about 10 keV. The achieved energy threshold level is 6 keV for our DSSDs. This is what enabled us to obtain the Compton image for such low energy gamma-rays.

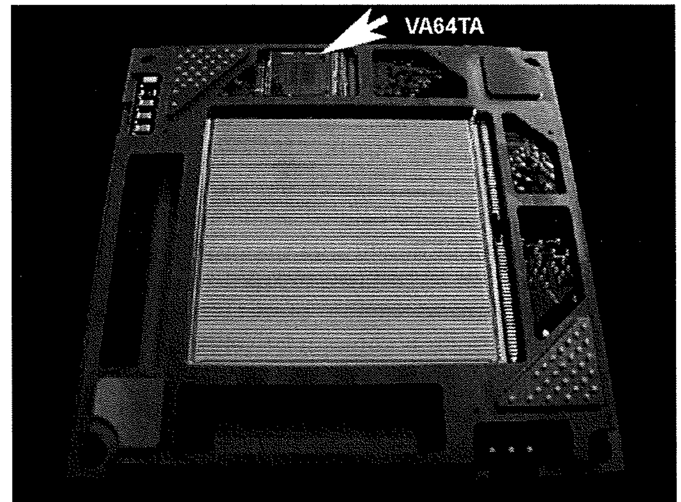
We have established a working model of the Si/CdTe semiconductor Compton camera concept with this prototype. The prototype experiment demonstrates that it is possible to build a Si/CdTe Compton camera that reaches the theoretical limit of angular resolution as a result of Doppler broadening. In response to the prototype results, we have set our goal: Si/CdTe semiconductor Compton cameras with a 1% energy resolution (ΔE(FWHM)$/E$), the Doppler-limited angular resolution and a 10% detection efficiency. In the following sections, we report our developments of DSSDs and CdTe pixel detectors for the next version of the Compton camera.

3. Development of a new DSSD stack

First of all, in order to improve the efficiency of Compton scattering, a tight stack of DSSDs is necessary. We therefore designed and constructed new DSSD modules to create a compact DSSD stack. Fig. 3 shows pictures of the DSSD module. The size of the DSSD is 2.56 cm × 2.56 cm with a thickness of 300 μm. The strip pitch is 400 μm. Each side has 64 strips and the signals from the strips are processed by new analog ASICs, VA64TAs, which were developed by this research team in conjunction with IDEAS. The VA64TA features low noise performance and low power consumption [5].

The stack pitch of 2 mm is available by using the DSSD modules. For 10% Compton efficiency, 40 layers of 300 μm thick DSSDs or 24 layers of 500 μm thick DSSDs are required [9,10]. It is essential to reduce the gap between the DSSD layers and to stack them tightly. If DSSDs are stacked loosely, the DSSD stack becomes too tall. In this case, too many CdTe detectors are needed to prevent the gamma-ray photons scattered in the DSSDs from escaping.

It is also important to reduce material around the DSSDs for effective detections of low energy (~100 keV) gamma-ray in the Compton camera. The gamma-ray photons scattered in DSSDs must reach an absorber detector directly without being scattered or absorbed. Therefore, we have used kapton plastic as the DSSD jig



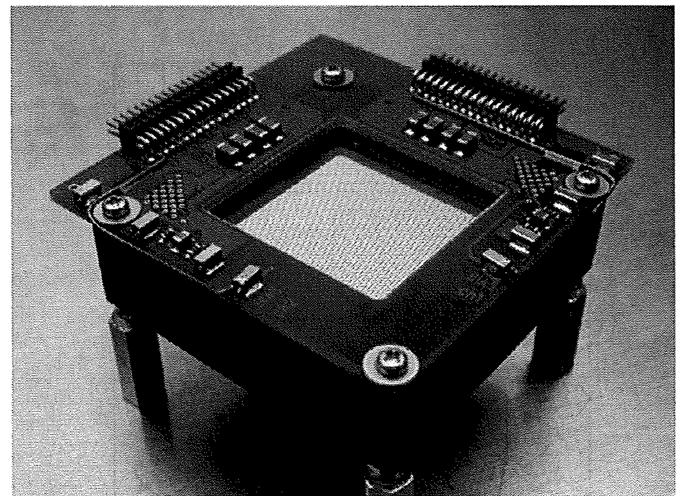


Fig. 3. The new DSSD module and the new DSSD stack. The size of the DSSD is 2.56 cm × 2.56 cm. The 0.3 mm thick DSSDs are stacked in four layers. The pitch between the layers is 2 mm.

material instead of the Al_2O_3 ceramic used in previous modules.

For the first step, we have stacked the DSSD modules in four layers and have tested the DSSD stack in photo-absorption mode by applying a bias voltage of 100 V between the P-side and the N-side. Fig. 4 shows gamma-ray spectra obtained with P-side strips. The average energy resolution from all P-side strips was 1.5 keV (FWHM) at 59.54 keV with an operating temperature of −10 °C. More details about the DSSD modules' properties are described in Takeda et al. [11].

4. CdTe Pixel detector module

In the Si/CdTe Compton camera, CdTe pixel detectors have to cover the DSSD stack with a large solid angle in order to absorb as many gamma-rays scattered in the DSSDs as possible. We designed a CdTe pixel detector module and constructed a number of these modules.

Fig. 5 shows the newly developed CdTe pixel module. The CdTe crystal is manufactured by ACRORAD in Japan

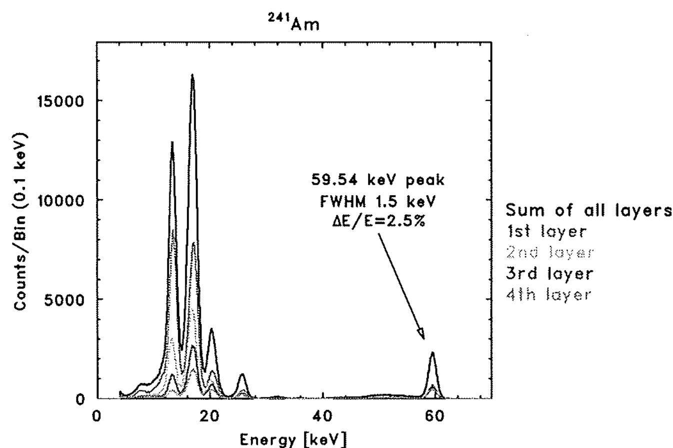


Fig. 4. ^{241}Am spectra obtained with the DSSD stack. The grays show spectra from the first layer, the second layer, the third layer and the fourth layer, respectively. The black spectrum shows the sum of all layers. The achieved energy resolution is 1.5 keV (FWHM) at 59.54 keV. The operating temperature is −10 °C.

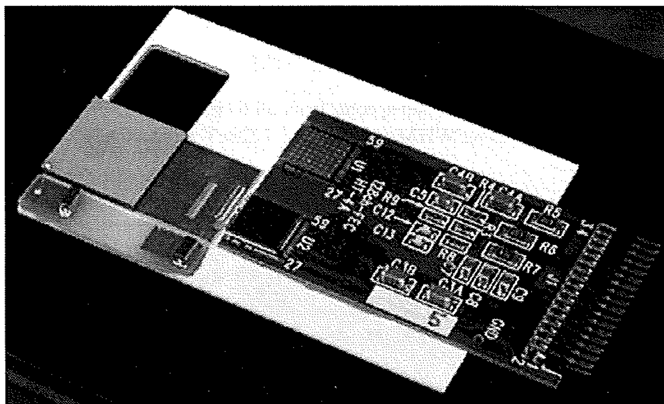


Fig. 5. The newly developed CdTe pixel detector module.

using the Traveling Heater Method. The size of the CdTe device is 13.35 mm × 13.35 mm and the thickness is 0.5 mm. This is a Schottky CdTe diode device, utilizing indium as the anode and platinum as the cathode [6,7,12,13]. The indium side is used as a common electrode, and the platinum side is divided into $8 \times 8 = 64$ pixels. The pixel size is 1.35 mm × 1.35 mm, and the gap between the pixel electrodes is 50 μm. Around the pixels, a guard ring electrode with a width of 1 mm is attached. This is attached so as to reduce leakage current, as most of the leakage current occurs through the device perimeter [14]. Additionally, a thin layer of gold is evaporated on the Pt side for the purpose of the ensuring good bump bonding connectivity.

In order to connect the pixels to the one-dimensional ASIC, a fanout board was designed. The substrate of the fanout board is made from a 96% Al_2O_3 ceramic with a thickness of 300 μm. The fanout board consists of bump pads, through-holes and patterns that route the signal from bump pads on both surfaces of the ceramic substrate.

Each pixel is connected to the bump pads on the fanout board by In/Au stud bump bonding technology, developed specifically for CdTe detectors [8]. A needle-shaped stud consisting of two stages of gold studs is fixed to the bump pad of the fanout board. The studs are made with a gold wire, and a thin layer of indium is printed on the top of the stud. There are 92 studs, including 64 for the pixels and 28 for the guard ring. The CdTe device and the fanout board are then pressed under controlled temperature conditions. In the previous design of the CdTe pixel detector, epoxy resin was used to fill in the space between the CdTe device and the fanout board. However, we found that epoxy resin degraded electrical resistance properties. Therefore, in this version, no epoxy resin was used. The mechanical strength of the module is still maintained, even without the use of epoxy resin.

Before wire bonding from the fanout board to the ASIC, we measured the leakage current. In our previous study, we found that the leakage current measurements of the detectors assist in the selection of good detectors [15]. The setup of the leakage current measurement is shown in Fig. 6. The sum leakage current of all 64 pixels and that of the guard ring were simultaneously measured separately. By bringing a probe into contact with the through hole on the ceramic fanout board, the pixel electrode side can be accessed without damaging the electrodes. We took the I-V curve up to 700 V and the time variation of the leakage current under a bias voltage of 700 V at a temperature of 20 °C. We then performed the selections to build up the pixel modules. The selection criterion is that the leakage current under the bias voltage of 700 V must be stable. This is, any variance must remain within a 10% variation range for a period of two hours.

We measured the leakage currents of 106 bump bonded CdTe devices and selected 74 devices from these. The distribution of the leakage currents for the pixels under a bias voltage of 700 V in a temperature of 20 °C approximated the Landau distribution. The most probable value was 1.2 nA and the sigma was 0.19 nA. Each selected device was wire bonded to a VA64TA. CdTe pixel modules were then created from the selected devices.

We tested the pixel modules by irradiating them with gamma-rays from radio isotopes. Fig. 7 shows ^{241}Am and ^{57}Co spectra obtained from one of the CdTe pixel detector

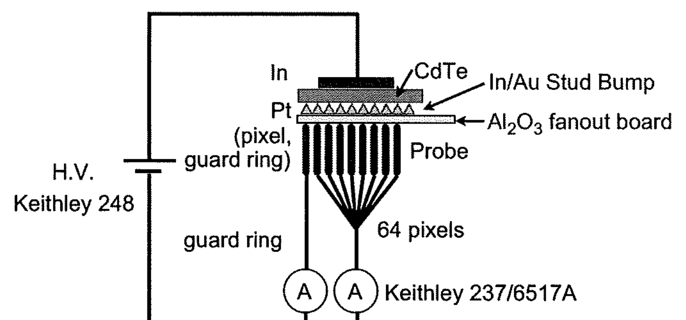


Fig. 6. The setup of the leakage current measurement.