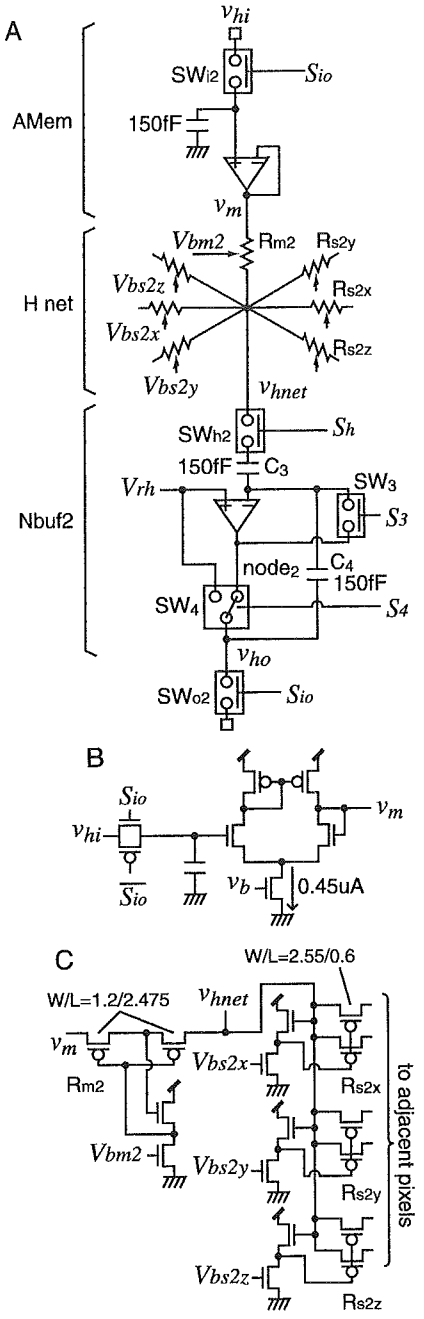

Fig. 3. A: Circuit design depicting the single pixel of the horizontal cell network chip (H chip). The pixel circuit consists of an analog memory (AMem), a resistive network (H net), and a S/H circuit (Nbuf2). B: Detailed design of the AMem. A current applied to the AMem is 0.45 μA and is much less than that applied to the Nbuf2. C: Detailed design of the H net. The H net is controlled separately by four MOS resistors: R_{m2}, R_{s2x}, R_{s2y}, and R_{s2z}. Therefore, an extent of smoothing and an orientation of electrical coupling are controlled by bias voltages, V_{bm2}, V_{bs2x}, V_{bs2y}, and V_{bs2z}. The Nbuf2 is the same design as the Nbuf1 of the P chip.

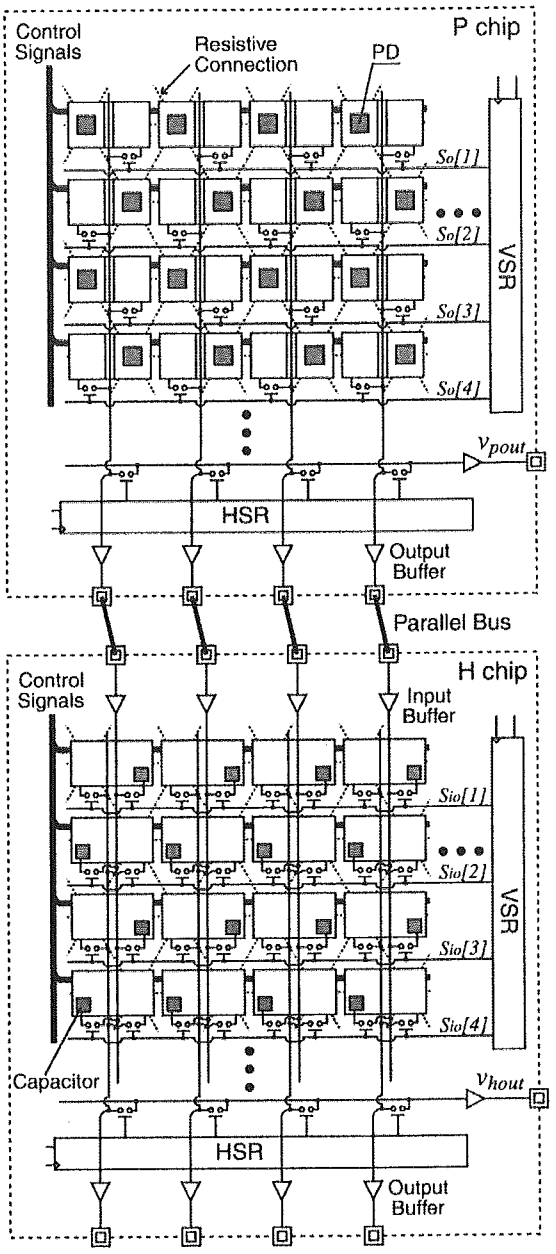

Fig. 4. Block diagrams of the photoreceptor network chip (P chip: top) and the horizontal network chip (H chip: bottom). These chips consist of a pixel array, VSR (vertical shift register), HSR (vertical shift register), and line parallel input/output buffers. In the P chip, the photo-diodes (PD: shadowed) are arranged on a hexagonal grid. The P and H chips are connected by a parallel bus. Each row of output selected by the VSR of the P chip is transferred to a corresponding row of the H chip pixel array through the parallel bus. Outputs of the P and H chips are read, pixel by pixel, by the VSR, and HSR.

transferred through a parallel bus simultaneously [26]. The line parallel transfer is carried out by the input and output buffers, which are voltage followers with wide range amplifiers. A current applied to the I/O buffer is about 50 μA, in order to drive I/O pads and the transfer bus quickly. Due to the line parallel transfer, the transfer time for one frame takes only less than 100 μs. In the H chip, each pixel is connected to neighboring ones by MOS resistors. The spatial arrangement of pixels is the same as that of the P chip. The image processing can be carried out with externally applied control signals—in this case, generated by a FPGA.

B. Operation of the Line Parallel Data Transfer

The voltages transferred through the separate transfer path in parallel are degraded by the pattern noise due to the statistical mismatch of circuit elements. Fig. 5 shows a schematic diagram of a single transfer path connecting a P chip pixel and corresponding H chip pixel. Circuit elements relevant to the source of the fixed pattern noise on the transfer path are the output buffer in the P chip, the input buffer in the H chip, the analog memory

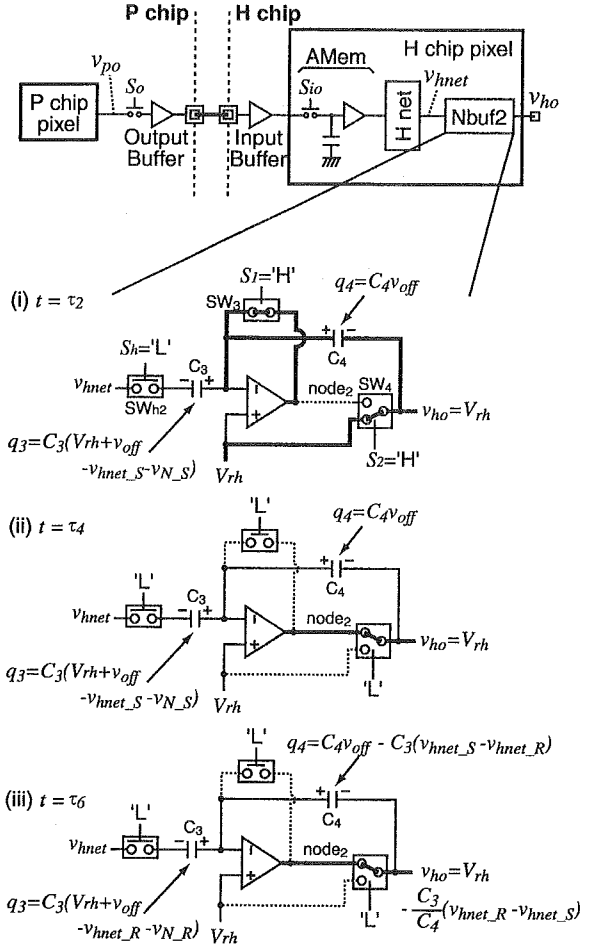

Fig. 5. Schematic diagram of one transfer path from a P chip pixel to (top) an H chip pixel. The left and right rectangles show the P chip pixel and the corresponding H chip pixel, respectively. The bottom shows states of the Nbuf2 at major times of the operation for image transfer in Fig. 6.

buffer in the H chip and the H chip resistive network. In our multichip silicon retina, Nbuf2 of Fig. 3, compensates for the pattern noise.

Fig. 6 demonstrates an operation of the data transfer from the P chip to the H chip. During the period of (A), the output voltage of a P chip pixel, $v_{\rm po}$ of Fig. 2, is obtained as [1]

$$v_{\rm po}(\tau_0) = -\frac{C_1}{C_2}\Delta v_{\rm pnet} + V_{\rm rp} \tag{1}$$

where

$$C_1 = C_2.$$

Here, $\Delta v_{\rm pnet}$ is the light-induced voltage change of the P chip resistive network during the accumulation time. Note that the output voltage of the P chip, $v_{\rm po}$, does not contain fixed-pattern noise occurring in the APS, the P chip resistive network nor the offset of the Nbuf1 since the noise is compensated for by the S/H circuit of the P chip [1]. During the same period, the $\rm SW_{o1}$ of Fig. 2 and $\rm SW_{i2}$ of Fig. 3 are closed to transfer the P chip pixel voltage, $v_{\rm po}(\tau_0)$, to the analog memory of the H chip (read operation), and then disconnected to hold the voltage (write operation). The voltage of the analog memory is smoothed by the

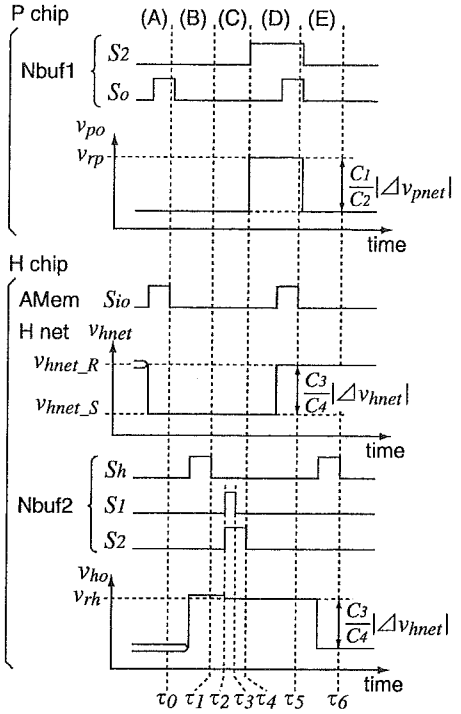

Fig. 6. Operation of data transfer between the P and H chips. Transitions of major responses and control signals on the transfer path are indicated.

H chip resistive network. The smoothed output of the H chip resistive network, $v_{\rm hnet}(\tau_0)$ of Fig. 3, is expressed as

$$v_{\rm hnet}(\tau_0) = v_{\rm hnet\_S} + v_{N\_S}$$

where v_{N_S} is the pattern noise component induced in the transfer path including the output buffer of the P chip, the input buffer of the H chip, the analog memory of the H chip and the H chip resistive network. $v_{\rm hnet\_S}$ represents an image of the H chip resistive network.

At t $= \tau_1$, the $\rm SW_{h2}$ of Fig. 3 is closed to sample $v_{\rm hnet}(\tau_0)$ in the capacitor $\rm C_3$ of Nbuf2, and then disconnected to hold the voltage. This operation is referred to as a sample operation. During the period of (C), an output of the Nbuf2 is reset to the reference voltage $V_{\rm rh}$ as follows. At first, the $\rm SW_3$ of Fig. 3 is closed and the $\rm SW_4$ of Fig. 3 is connected to $V_{\rm rh}$ at t $= \tau_2$ and then the $\rm SW_3$ is opened again at t $= \tau_3$. Here, the inverting node of the Nbuf2 becomes floating and the accumulated charges q_3 and q_4 at t $= \tau_2$ are preserved in the capacitors $\rm C_3$ and $\rm C_4$, respectively. Next, the $\rm SW_4$ is connected to the amplifier output, $\rm node_2$ at t $= \tau_4$. Fig. 5(i) and (ii) shows the states of the Nbuf2 at t $= \tau_2$ and τ_4, respectively. In these cases, the inverting input node voltage of the amplifier v_- is

$$v_- = V_{\rm rh} + v_{\rm off}$$

where $v_{\rm off}$ is an offset of the Nbuf2. Therefore, the accumulated charges of the capacitors $\rm C_3$ and $\rm C_4$ at t $= \tau_4$ are expressed as

$$q_3(\tau_4) = C_3(V_{\rm rh} + v_{\rm off} - v_{\rm hnet\_S} - v_{N\_S}) \tag{2}$$

$$q_4(\tau_4) = C_4 v_{\rm off} \tag{3}$$

respectively. Equations (2) and (3) show that these capacitors store the image signal of the H chip resistive network at t $= \tau_0$,

the pattern noise components and the offset of the Nbuf2. This operation is referred to as a reset operation.

During the period of (D), the output voltage of the P chip pixel, $v_{\rm po}$, is fixed to the reference voltage, $V_{\rm rp}$, for all pixels. This operation is carried out by connecting the SW_2 of the Nbuf1 to $V_{\rm rp}$ without destructing the P chip image signal, since C_1 and C_2 of the Nbuf1 hold the image signal. During this period, the SW_{o1} and SW_{o2} are closed and the reference voltage of the P chip pixel is transferred to and stored in the analog memory of its corresponding H chip pixel. The SW_{o1} and SW_{o2} are opened at $t = \tau_5$ (these operations are referred to as read and write operations of reference voltage). Accordingly, the reference voltage of the H chip resistive network, $v_{\rm hnet}(\tau_5)$, is varied to

$$v_{\rm hnet}(\tau_5) = v_{\rm hnet\_R} + v_{N\_R}.$$

Here, v_{N_R} is the pattern noise component occurring in the transfer path as v_{N_S}. $v_{\rm hnet\_R}$ is the voltage of the H chip resistive network measured when $V_{\rm rp}$, the reference voltage of the Nbuf1 of Pchip, is fed in.

During the period of (E), the SW_{h2} is closed again to memorize the reference voltage of the H chip resistive network, $v_{\rm hnet}(\tau_5)$, in C_3 of Nbuf2, and is then disconnected to hold the voltage at $t = \tau_6$ [this is the same as the sample operation during the period of (B)]. Fig. 5(iii) shows the state of Nbuf2 at $t = \tau_6$. The accumulating charge q_3 at $t = \tau_6$ is expressed as

$$q_3(\tau_6) = C_3(V_{\rm rh} + v_{\rm off} - v_{\rm hnet\_R} - v_{N\_R}). \quad (4)$$

The difference between $q_3(\tau_4)$ and $q_3(\tau_6)$ is accumulated in the capacitor C_4. The accumulated charge q_4 at $t = \tau_6$ is expressed as

$$\begin{aligned} q_4(\tau_6) &= q_4(\tau_4) + q_3(\tau_4) - q_3(\tau_6) \\ &= C_4 v_{\rm off} - C_3(v_{\rm hnet\_S} - v_{\rm hnet\_R}) \end{aligned} \quad (5)$$

because v_{N_R} is equal to v_{N_S}. Therefore, the output voltage of the H chip pixel of Fig. 3, $v_{\rm ho}$, is expressed as

$$\begin{aligned} v_{ho}(\tau_6) &= v_{-} - \frac{q_4(\tau_6)}{C_4} \\ &= -\frac{C_3}{C_4}(v_{\rm hnet\_R} - v_{\rm hnet\_S}) + V_{\rm rh} \\ &= -\frac{C_3}{C_4}\Delta v_{\rm hnet} + V_{\rm rh} \end{aligned} \quad (6)$$

where

$$C_3 = C_4.$$

Here, $\Delta v_{\rm hnet}$ represents the output image of the H chip smoothed by the resistive network, and does not contain the pattern noise nor the offset of the Nbuf2.

C. Specifications

The specifications of the multichip silicon retina (the P and H chips) and the single-chip silicon retina are shown in Table I. The multichip and single-chip silicon retinas were implemented with a 0.6 μm, double-poly, three-metal, standard CMOS technology and these die sizes were 8.9 x 8.9 mm^2. The P and H chips have 70 x 80 pixels. The pixel area of these chips was 103.5 x 89.6 μm. The photo diode area was 647.4 μm^2. As is clearly shown, the fill factor and the number of pixels have been improved significantly. The number of pixels has tripled, and the fill factor has more than doubled compared to the single-chip silicon retina. Note that the pixel area of the single-chip is larger than a total pixel area of the P and H chips although the pixel circuit of the single-chip is redistributed to the pixel circuits of the P and H chips with some additional circuits, which are the analog memory and the bias circuits of the H chip resistive network. We reduced wasted spaces and design margins in the pixel layout, which existed in the single-chip, as much as possible. The design margins of source and signal line width were improved. The reduction of the wasted spaces in the P and H chips was easier than in the single-chip because the pixel circuit of the P and H chips had less transistors and simpler design in terms of the hexagonal arrangement.

TABLE I
SPECIFICATIONS OF THE MULTICHIP AND SINGLE-CHIP SILICON RETINAS

	multichip	single-chip[1]
Process	CMOS 0.6um double poly three metal	
Die size [mm^2]	8.9 x 8.9	
Number of pixels [pixel]	70(H) x 80(V)	40(H) x 46(V)
Pixel area [um^2]	103.5 x 89.6 (= 9273.6) 2 : $\sqrt{3}$	178.7 x 154.7 (= 27644.9) 2 : $\sqrt{3}$
PD area [um^2]	647.4	868.0
Fill factor[%]	6.98	3.14
Transistor count/pixel	P chip : 34 H chip : 38	63
Power consumption [mW@3.3V]	P chip : 217.1 H chip : 217.8 - -	power saving off 367.9 power saving on 40.0
Read time [ms/frame]	serial : 3.4 parallel : 0.091	serial : 1.2 -

The power consumptions of the P and H chips were about 220 mW at 3.3-V power supply. These chips had no power-saving function embedded in the single-chip to reduce the power consumption. If the power-saving mode is active, current is not supplied to the S/H circuit array except for the S/H circuit in the row selected by the vertical shift register during a read time. The power-saving function in the single-chip reduced the power consumption to about one-ninth, as shown in Table I. The total power consumption of the P and H chips is the same level as that of the single-chip, although the number of pixels of the P and H chips was tripled. If the power-saving function is embedded in the P and H chips [1], the power consumption will be substantially reduced.

The read time of the P and H chips using a serial method took 3.4 ms and had tripled compared to the single-chip silicon retina due to the increase in pixel count. The read time, however, entailed no adverse consequences for real-time processing, because the read time is sufficiently shorter than the accumulation time of the APS (which is several tens of ms). Furthermore, the read time using a parallel method took only 91 μs. Thus, the line parallel method makes higher speed transfer possible between the chips comprising the multichip system.

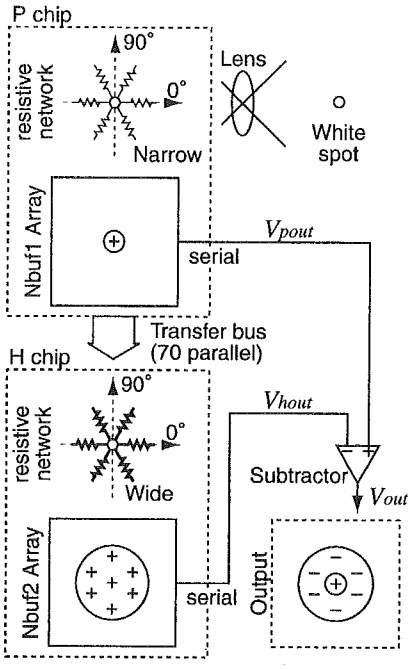

Fig. 7. System design of the multichip silicon retina. The system consists of the P chip, the H chip, and an off-chip subtractor. Two dotted rectangles show the (top) P chip and (bottom) the H chip. In the dotted rectangle, six resistors represent resistances between adjacent pixels at 0°, 60°, and 120° in the resistive network, and wider line represents lower resistance. A square in the dotted rectangle is a processed and stored image in the Nbuf(1,2) array and "+" and "−" represent a positive and negative responses compared with a baseline voltage, respectively.

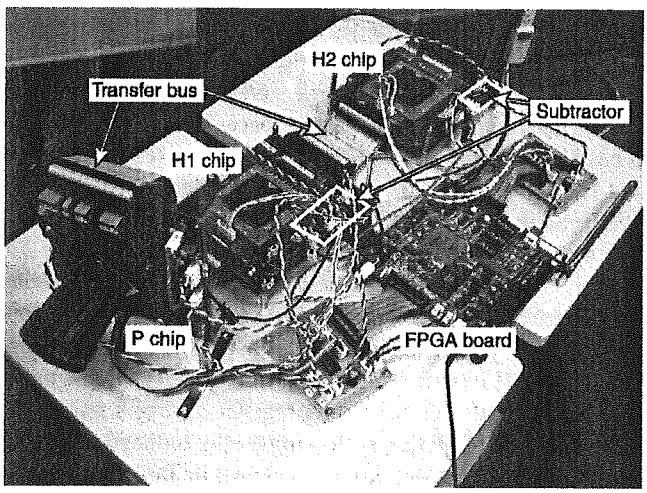

Fig. 8. Overview of the multichip system. In this case, the system consists of a P chip board, two H chip boards, and a FPGA board. Each of the chip boards has the off-chip subtractor. These chip boards are connected by a wire harness.

III. Center-Surround Receptive Field of Multichip Silicon Retina

The multichip silicon retina was configured as illustrated in Fig. 7. A camera lens was mounted on the P chip. The P and H chips were connected by a transfer bus consisting of 70 parallel lines. Output voltages of corresponding pixels in the P and H chips were read out simultaneously and their voltage difference was obtained through an off-chip differencing circuit (subtractor). Fig. 8 shows an overview of the multichip silicon retina. A wire harness was used as the transfer bus. Each chip was controlled by FPGA logic.

The center-surround receptive field of the multichip silicon retina is obtained as follows. First, the APS array outputs a light-induced image for a white spot. The image is smoothed weakly by the resistive network of the P chip. The weakly smoothed image is sampled and held in the Nbuf1 array by the sample operation as in the period (B) of Fig. 6. The Nbuf1 array is reset to output $v_{\rm rp}$ by the reset operation as in the period (C) of Fig. 6. Then, the APS array is initialized by setting S_p high. The initialized voltage of the P chip resistive network is sampled and held in the Nbuf1 array as reference voltage, and is used in pattern noise compensation by the sample operation as in the period of (E) of Fig. 6. Thus, the weakly smoothed spot image is stored in the Nbuf1 array without being influenced by the pattern noise components.

Second, by the same operation as in Section II-B, the weakly smoothed spot image of the P chip is transferred to the H chip through the line parallel transfer bus by vertical shift register, and is smoothed strongly by the wide receptive field produced by the H chip resistive network. The strongly smoothed image is stored in the Nbuf2 array and is not influenced by the pattern noise components.

Finally, the outputs of the P and H chips are read successively by horizontal and vertical shift registers, and are fed directly into the off-chip subtractor at the same timing. The output of the subtractor $V_{\rm out}$ is expressed as

$$V_{\rm out} = V_{\rm pout} - V_{\rm hout}. \tag{7}$$

This is the difference between the outputs of the two resistive networks. The distribution of $V_{\rm out}$ exhibits the center-surround antagonistic response to the spot image. The receptive field is approximated by the $\nabla^2 G$ filter. Here, the processing speed of the subtractor is sufficiently faster than the read speed of these chips. Therefore, the subtractor allows real-time processing at the same time as the read operation without time delay. The processing time of the multichip silicon retina containing the transfer time is about 3.6 ms, and is less than the accumulation time; therefore, the system can realize real-time processing.

A. Response to a Black-White Edge

To examine the properties of the center-surround receptive field quantitatively, the voltage response of the multichip silicon retina to a black-white edge was measured. Fig. 9 shows the responses of the P chip (A), the H chip (B), and the off-chip subtractor (C) to the black–white image. The location of the introduced pattern is shown on the top of the figures. The experiment was carried out under indoor illumination (0.65 [W/m^2]). The accumulation time of the photo-sensors was 15.0 ms. The bias voltage applied to the resistive network of the P chip, $V_{\rm bs1}$, was 0.50 V. The bias voltage applied to the resistive network of the H chip $V_{{\rm bs2}\{x,y,z\}}$ varied from 0.45 to 0.85 V. In these figures, the horizontal axis measures the pixel position and the vertical axis measures the pixel voltage of the 40th row of each chip.

As shown in Fig. 9(A), the voltage dropped about 400 mV within six pixels from the black region to the white region. This

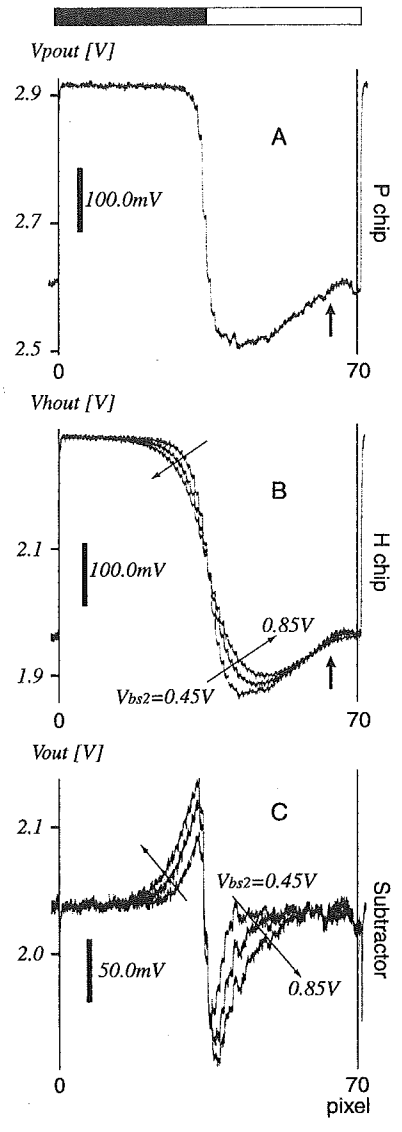

Fig. 9. Responses to a black-white edge obtained from (A) the P chip, (B) the H chip, and (C) the subtractor. The top shows the black-white image presented to the P chip. $V_{\mathrm{bs2}\{x,y,z\}}$ was varied from 0.45 to 0.85 V in the directions of the arrows.

indicates that the edge of the black-white edge was slightly blurred, since the neighboring pixels of the P chip are weakly coupled. The fluctuation of voltage due to the pattern noise was suppressed within 5mV of the black region and 10 mV of the white region with the aid of the S/H circuits. On contrast, the border was strongly blurred in the H chip [Fig. 9(B)]. The fluctuation of voltage is smaller than that of the P chip due to the smoothing effect of the tight electrical coupling between neighboring pixels in the H chip. The border is blurred more as $V_{\mathrm{bs2}\{x,y,z\}}$ is increased because the resistance connecting the neighboring pixels decreases.

The output of the subtractor shows a Mach band-like effect near the black-white border as shown in Fig. 9(C). The receptive field size becomes wider and the response amplitude becomes larger when the resistance of the H chip, R_{s2} of Fig. 3, is decreased by increasing $V_{\mathrm{bs2}\{x,y,z\}}$ [19], [27]. These properties are thought to be relevant to a part of the neural dark adaptation controlled by the IP cell [28]. The fluctuation is larger in the

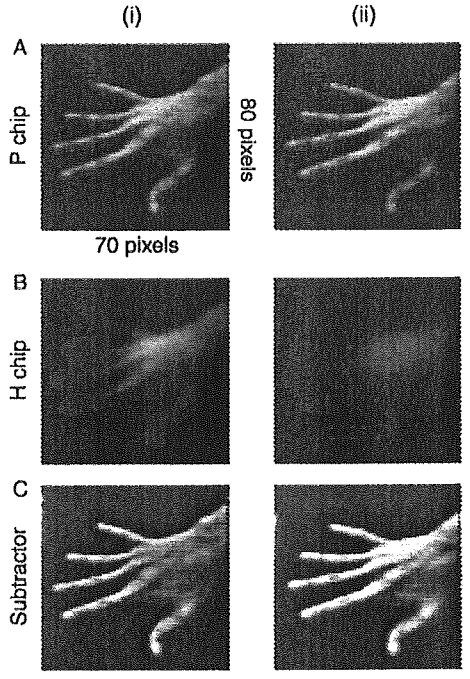

Fig. 10. Responses to a hand obtained from (A) the P chip, (B) the H chip, and (C) the subtractor. The images in column (i) were obtained when $V_{\mathrm{bs2}\{x,y,z\}}$ is 0.45 V, and the images in column (ii) were obtained when $V_{\mathrm{bs2}\{x,y,z\}}$ is 0.85 V.

white region but suppressed within 10 mV. A gradual decrease of the amplitude (upward decline indicated by arrows) is seen. The reason for this phenomenon is probably a light falloff or a vignetting due to the mounted lens.

Fig. 10 shows the responses to a hand obtained from the P chip (A), the H chip (B), and the subtractor (C). The hand was presented on a black background. The experiment was carried out under indoor illumination (0.48 [W/m^2]). The accumulation time of the photo sensors was 33.3 ms. In this case, the bias voltage of the P chip V_{bs1} is 0.0 V and the MOS resistor has high impedance to decouple the neighboring pixels. The images in column (i) were obtained when the bias voltage of the H chip, $V_{\mathrm{bs2}\{x,y,z\}}$, was 0.45 V and the images in column (ii) were obtained when $V_{\mathrm{bs2}\{x,y,z\}}$ was 0.85 V. The responses were displayed with a PC through an interface board. As shown in A-(i) and A-(ii), the hand is clearly captured by the P chip. In contrast, the H chip outputs strongly blurred images as shown in B-(i) and B-(ii). In B-(ii), the image is blurred more strongly and the fingers of the hand are not discernible. C-(i) and C-(ii) show subtraction between these output images and exhibit clear Mach band-like effects around the contour of the hand, indicating that the multichip silicon retina possesses a ∇^2G-like receptive field. The contour of the hand is enhanced more prominently and the output voltages are smaller in C-(i) than in C-(ii).

B. Effects of Offset Compensation

We verified the effects of the S/H circuit in offset compensation. Statistical mismatch of the transistor characteristics is a bottleneck in the design of analog silicon retinas [3], [29], [30]. The mismatch yields a pattern noise such as the fixed-pattern noise of a photo-sensor [31] and the offset of the amplifier [3]. As a result, the output voltages of the silicon retina become seriously degraded [3]. To compensate for the pattern noise of the

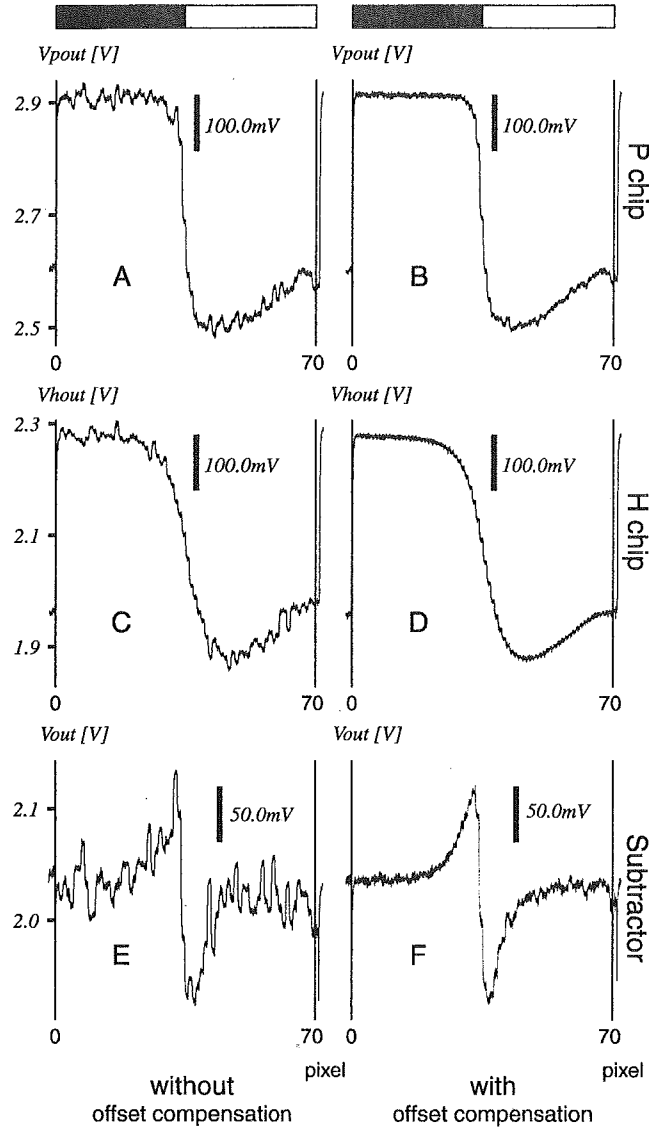

Fig. 11. Effects of offset compensation on the multichip silicon retina. These responses were obtained from (top) the P chip, (middle) the H chip, and (bottom) the subtractor. B, D, and F show the responses obtained when the offset compensation is activated.

P chip, SW_1 is opened first and then SW_2 is connected to the amplifier output, $node_1$ (Fig. 2). The offset compensation can be deactivated by changing the control sequence. Namely, SW_2 is connected to $node_1$ first and then SW_1 is opened. In this case, (1) becomes

$$v_{\rm po} = -\Delta v_{\rm pnet} + V_{\rm rp} + v_{\rm off1}.$$

Here, the offset in Nbuf1 $v_{\rm off1}$ remains. By controlling Nbuf2 in a similar way, (6) becomes

$$v_{\rm ho} = -\Delta v_{\rm hnet} + V_{\rm rh} + v_{\rm off2}.$$

Here, the offset in Nbuf2 $v_{\rm off2}$ remains.

In Fig. 11, the output voltage of the P chip (A and B), the H chip (C and D), and the subtractor (E and F) in response to a black-white edge are shown to examine the effects of offset compensations. The introduced pattern is illustrated on the top. The experiment was carried out under indoor illumination (0.65 [W/m^2]). The accumulation time of the photo-sensors was 15.0 ms. The bias voltage applied to the resistive network of the P chip $V_{\rm bs1}$ was 0.50 V and to the resistive network of the H chip $V_{{\rm bs2}\{x,y,z\}}$ was 0.65 V. In these figures, the horizontal axis measures the pixel position and the vertical axis shows the corresponding pixel voltage of the 40th row of each chip.

Fig. 11(A) and (B) shows the output voltages of the P chip obtained when the offset compensation was deactivated and activated, respectively. As shown in Fig. 11(A), when the compensation was deactivated, the output voltage fluctuates due to the variation of the offset among Nbuf1s. The fluctuation reaches about 40 mV. In contrast, when the compensation was activated as shown in Fig. 11(B), the fluctuation due to the offset was suppressed below 5 mV in the black region. The fluctuation was relatively large in the white region compared to the black region, indicating the gain mismatch among APSs. In this design, this gain mismatch cannot be compensated for; however, the fluctuation caused by the gain mismatch is not as prominent as that caused by the offset.

Fig. 11(C) and (D) shows the output voltages of the H chip. The offset compensation was activated in the P chip in this measurement. Fig. 11(C) was obtained when the offset compensation in the H chip was deactivated, and Fig. 11(D) was obtained when the offset compensation in the H chip was activated. The fluctuation of the voltage among the pixels was prominently reduced below 2 mV by the offset compensation in the H chip. The fluctuation level of the H chip is smaller than that of the P chip due to the tight electrical coupling between the neighboring pixels in the H chip. The voltage fluctuation of the H chip did not change, even when the offset compensation was deactivated in the P chip (not shown). This also suggests that the fluctuation of the P chip output shown in A is smoothed out by the tight electrical coupling among H chip pixels.

Fig. 11(E) shows the output voltage of the subtractor obtained when the offset compensation is deactivated in both chips. Fig. 11(F) shows the output voltage obtained when the compensation is activated in both the P and H chips. When the offset compensation was deactivated in both chips, the fluctuations reached 65 mV at a maximum. In contrast, when the compensation was activated on both chips, the fluctuation in the black region had been drastically reduced to below 5 mV, and those in the white region below 10 mV. These results indicate that the pattern noise due to the amplifier offsets is effectively compensated for by the S/H circuit.

The pattern noise arises, however, from the fixed pattern noise of the APS, the offset of the line parallel I/O buffer, the mismatch of the transistors in the MOS resistors and switches other than the amplifier offsets. Therefore, the signal-to-noise ratio would be worse if the S/H circuits in the chip were completely removed.

C. Chip Response With Different Accumulation Times

In Fig. 12, the responses of the photo sensor with different accumulation times are shown. Fig. 12(A)–(C) shows the responses of the P chip, the H chip and the subtractor, respectively. The introduced pattern is the black-white paper, as shown at the top. The experiment was carried out under indoor illumination

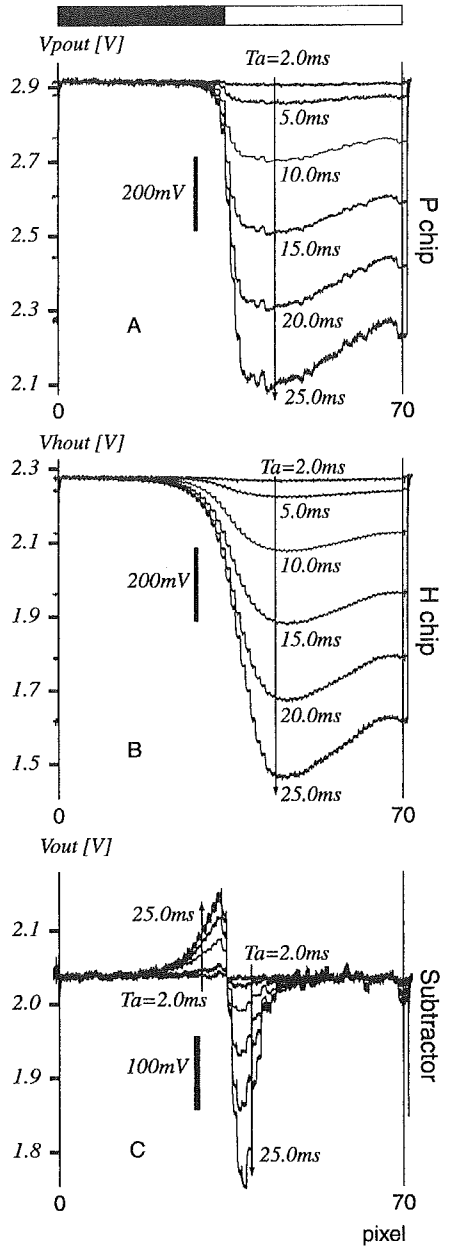

Fig. 12. Responses with different accumulating durations obtained from the (A) P chip, (B) the H chip, and (C) the subtractor. The accumulation time T_a was changed from 2.0 to 25.0 ms in the directions of the arrows.

(0.65 [W/m^2]). The accumulation time, T_a, was changed from 2.0 to 25.0 ms. In these figures, the horizontal axis measures the pixel position and the vertical axis measures the corresponding voltage output of the 40th row. As shown in Fig. 12(A) and (B), the voltage drops of the P and H chips in the white region become larger as the accumulation time is increased. The increase of the voltage drop is relatively linear with respect to the intensity of light within these accumulation times. As shown in Fig. 12(C), the response of the subtractor also increases as the accumulation time increased. However, the amplitude of the response is asymmetric to the border of the black-white image. This is because the resistance of the MOS resistor varies with the bias voltage of the input terminal. The current of the MOS resistor increases nonlinearly by the body effect as the bias voltage level of the terminal increases even if the potential difference

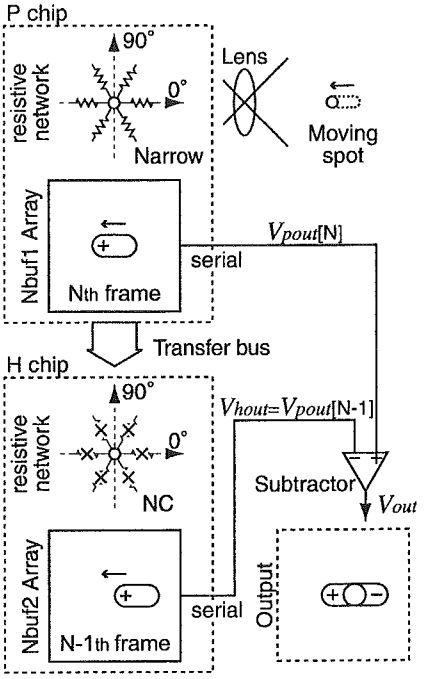

Fig. 13. System design for the frame subtraction. The system is the same configuration as the multichip silicon retina. A "×" on the resistance in the H chip square represents that the resistance has high impedance. The H chip serves as a frame memory when the resistances of $R_{s2\{x,y,z\}}$ have high impedance.

between two input terminals of the MOS resistor remains constant. Therefore, the space constant of the resistive network is different between the black and white regions. The baseline of the subtractor's response, however, does not change regardless of the accumulation time.

IV. Application

The advantage of the present multichip silicon retina is not limited to the improvement of pixel resolution. Some useful spatiotemporal filtering functions can be achieved with the multichip system by changing the control signal and the chip configuration.

A. Frame Subtraction

The detection (or segmentation) of moving objects is a basic task of computer vision. Frame subtraction is a standard technique for motion detection. Namely, subtraction of the current frame from the previous frame will remove most of the static background and extract only moving objects. The motion detection chips using the frame subtraction technique have been fabricated [20], [32] including the single-chip silicon retina of our previous study. The multichip silicon retina can also perform the frame subtraction using the same configuration as the ∇^2G-like filtering in the Section III.

Fig. 13 shows a system design for frame subtraction. The system consists of the P chip, the H chip, and the subtractor. The P chip outputs the current frame image and transfers to the H chip under which the bias voltage $V_{bs2\{x,y,z\}}$ of the H chip is 0.0 V so that the MOS resistor $R_{s2\{x,y,z\}}$ decouples the neighboring pixels. In this condition, the H chip serves as a frame memory that stores the previous frame image of the P chip. The

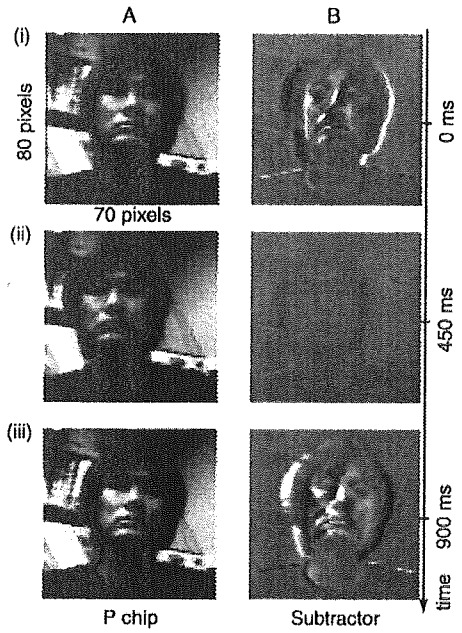

Fig. 14. Responses to a moving face obtained from (A) the P chip and (B) the subtractor by the frame subtraction. Times obtained with these images are indicated on the right side.

current and previous images are read out from these chips sequentially at the same timing and the frame subtraction is obtained through the off-chip subtractor.

Fig. 14 shows the response to a face obtained by the frame subtraction operation. The experiment was carried out under the same conditions as Fig. 10. The accumulation time of the photo sensors was 50 ms. In this case, the bias voltage of the P chip, $V_{\rm bs1}$, was 0.0 V. The face was moved right and left in front of the lens mounted on the chip. Each frame represents output images of the P chip and the subtractor picked up once every nine frames at a time indicated right side. The face was moving from right to left at 0 and 450 ms, and from right to left at 450 to 900 ms. At the time that the face was moving (0 and 900 ms), the moving face image of the subtractor was represented and the static background disappeared. And at the time that the face almost stopped (450 ms), the face image also disappeared.

B. Odd-Symmetric Orientation Selective Filter

In the digital image processing, the Sobel operator performs discrete differentiation on the image using small conventional masks to approximate the first derivative [33]. This operator takes the derivative in one direction, and smoothes in the orthogonal direction and is designed to respond maximally to edges running along the direction of smoothing.

A Sobel-like odd-symmetric receptive field is obtained by the multichip silicon retina. Fig. 15 shows a system design for the Sobel-like filtering. In Fig. 15, $V_{h1\rm out}(i,j)$ and $V_{h2\rm out}(i,j)$ are the output voltage of the pixel at (i, j) from the H1 chip and H2 chip, respectively. The system consists of the P chip, two H chips (H1 chip and H2 chip) and the subtractor. The H1 chip smoothes the image obtained from the P chip by the resistive network connected at one of three orientations. The H2 chip stores the elongated image of the H1 chip, without smoothing by the resistive network of the H2 chip. Thus, the H1 and H2 chips store the same image. The H1 and H2 chips output the elongated images

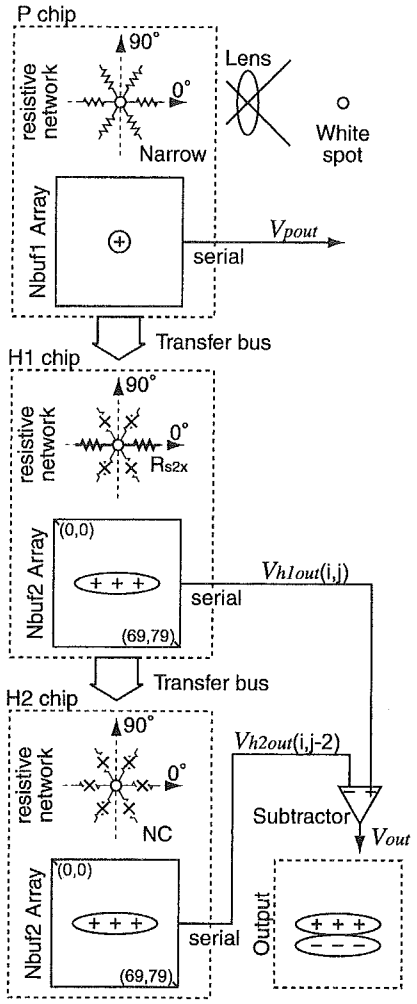

Fig. 15. System design for the Sobel-like odd-symmetric orientation selective filter. The system consists of the P chip, two H chips, and the off-chip subtractor.

to the off-chip subtractor sequentially. However, the timing of the readout in the H2 chip delays by a few columns and/or rows (two rows in this case), and outputs $V_{h1\rm out(i,j-2)}$. Accordingly, the subtractor takes the derivative in one direction and the output of the subtractor is

$$V_{\rm out}(i,j-1) = V_{h1\rm out}(i,j) - V_{h1\rm out}(i,j-2). \quad (8)$$

This is the difference between the jth and $(j-2)$th row of the image elongated at horizontal orientation. Thus, the multichip system takes the derivative in the vertical direction and smoothes in the horizontal direction. The filter property is similar to the Sobel operator, since the smoothing function by the resistive network is approximated by the exponential function. Note that the filter size is easily controllable by modulating the bias voltage of the resistive network and the readout timing of the H2 chip. The processing time of the Sobel-like filtering including the transfer time is about 3.8 ms and is less than the accumulation time.

Fig. 16 shows the responses of the P chip (A) and the H2 chip (B and C) obtained by the Sobel-like operation. Fig. 16(B) shows the responses obtained when the resistive network of the H1 chip was connected at 0° and the timing of the H2 chip readout was delayed by two rows. Fig. 16(C) shows the responses obtained when the resistive network of the H1 chip was

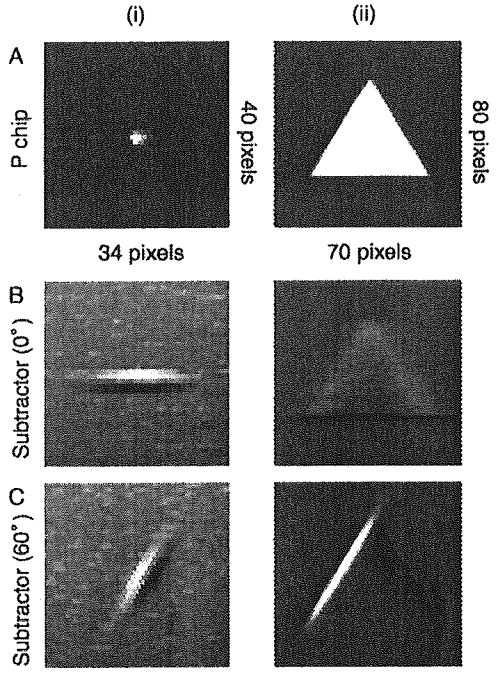

Fig. 16. Responses of the Sobel-like first derivative filtering to (i) a white spot and (ii) an equilateral triangle. A shows the responses obtained from the P chip. B and C show the responses obtained when the H net of the H1 chip was connected at 0° and 60° and the timing of the H2 chip readout was delayed by two rows and columns, respectively.

connected at 60° and the readout timing of the H2 chip was delayed by two columns. The images in column (i) were obtained when a white spot on a black background was presented, and the images in column (ii) were obtained when a equilateral triangle on a black background was presented. The experiment was carried out under indoor illumination (0.48 [W/m^2]). The accumulation time was 33.3 ms. The bias voltage of the P chip $V_{\rm bs1}$ was 0.0 V, and the bias voltage of the H1 chip $V_{\rm bs2x}$ or $V_{\rm bs2y}$ was 0.85 V. As shown in Fig. 16(B)-(i) and (C)-(i), elongated responses are arranged odd-symmetrically at 0° and 60° orientations, respectively. As shown in Fig. 16(B)-(i) and (B)-(ii), only one side of the triangle matching the preferred orientation is extracted while the other sides are blurred.

C. Even-Symmetric Orientation Selective Filter

An even-symmetric derivative filter can be also obtained with the multichip silicon retina. The center-surround receptive fields are smoothed for one orientation by two separate resistive networks and then the difference of these receptive fields is obtained by the subtractor. Fig. 17 shows a system design for even-symmetric orientation selective filtering. The system consists of a P chip and two H chips (H1 chip and H2 chip). The H1 chip outputs the center-surround responses generated with and without resistive coupling to the H2 chip in sequential order. The H2 chip smoothes these responses by the resistive network connected at one orientation and subtracts these elongated responses by the Nbuf2 array.

Fig. 17 demonstrates the operation for an even-symmetric receptive field oriented at 60°. The P chip takes a white spot image in order to indicate a receptive field of the system. First, the weakly smoothed spot image is stored in the Nbuf1 array.

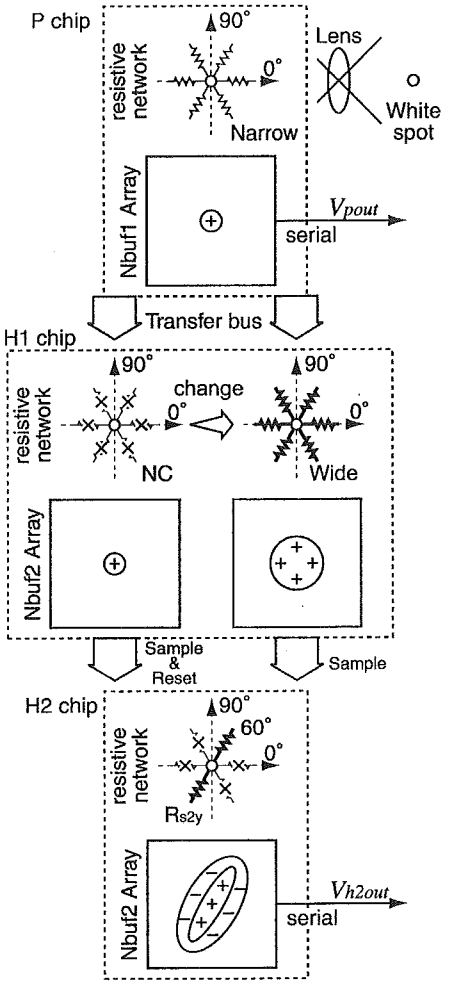

Fig. 17. System design for even-symmetric orientation selective filtering. The system consists of a P chip and two H chips. The H1 chip processes twice the image transfered from the P chip by changing the resistances, $R_{s2\{x,y,z\}}$ and the processed images are transferred to the H2 chip. The H2 chip smoothes these images at one orientation and takes a difference between these elongated images.

Second, using the same operation as in Section II-B, the weakly smoothed spot image of the P chip is transferred to the H1 chip through the line parallel transfer bus by vertical shift registor. Here, the bias voltage $V_{\rm bs2\{x,y,z\}}$ of the H1 chip is 0.0 V and the MOS resister, $R_{\rm s2\{x,y,z\}}$, decouples the neighboring pixels. Accordingly, the Nbuf2 array of the H1 chip stores the weakly smoothed image of the P chip.

Third, the H2 chip receives the image from the H1 chip and smoothes it at 60° by connecting the lateral MOS resistor $R_{\rm s2y}$ only. Therefore, a narrow and elongated image is produced by the H2 chip resistive network. Then, the Nbuf2 array of the H2 chip is reset while the narrow and elongated image is input by the sample and the reset operation. During the same period, and by the same operation as in Section II-B, the weakly smoothed spot image of the P chip is transferred again to the H1 chip. In this period, the image is smoothed strongly, because the receptive field of the H1 chip resistive network becomes wide due to the bias voltage $V_{\rm bs2\{x,y,z\}}$. Then, the Nbuf2 array of the H1 chip stores the strongly smoothed image.

Finally, the H2 chip receives the strongly smoothed image from the H1 chip and smoothes it at 60°. Therefore, a wide

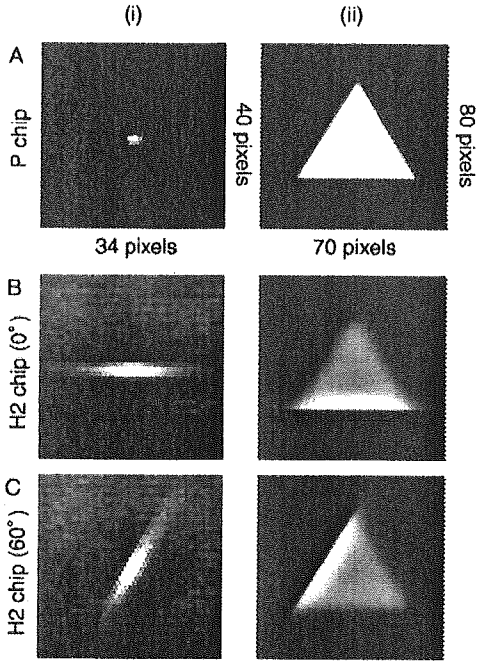

Fig. 18. Responses of the even-symmetric orientation selective filtering to (i) a white spot and (ii) an equilateral triangle. A shows the responses obtained from the P chip. B and C show the responses obtained when the H net of the H2 chip was connected at 0° and 60°.

and elongated image is produced by the H2 chip resistive network. Then, by the sample operation as the period (E) of Fig. 6, the Nbuf2 array of the H2 chip samples the wide and elongated image instead of a reference voltage. By this operation, the Nbuf2 array of the H2 chip can subtract the wide and elongated image from the narrow and elongated image under the compensation of pattern noise components. Therefore, an even-symmetric response oriented at 60° is obtained and stored in the Nbuf2 array of the H2 chip, without being influenced by the pattern noise. The processing time of the even-symmetric filtering, including the transfer time is about 3.9 ms, and is less than the accumulation time.

Fig. 18 shows orientation-selective responses by the even-symmetric filtering obtained from the P chip (A) and the H2 chip [(B) and (C)]. Fig. 18(B) and (C) shows the responses obtained when the resistive network of the H2 chip was connected at 0° and 60°, respectively. The images in column (i) were obtained when a white spot on a black background was presented. The images in column (ii) were obtained when an equilateral triangle on a black background was presented. The experiment was carried out under indoor illumination (0.48 [W/m^2]). The accumulation time was 33.3 ms. The bias voltage of the P chip V_{bs1} was 0.0 V. The bias voltage of the H1 chip $V_{\mathrm{bs2}\{x,y,z\}}$ was 0.65 V and the bias voltage of the H2 chip, $V_{\mathrm{bs2}x}$ or $V_{\mathrm{bs2}y}$, was 0.85 V. As shown in Fig. 18(B)-(i) and C-(i), even-symmetric impulse responses of the preferred orientation at 0° and 60° are exhibited, respectively, since there are positive narrow and elongated responses in the center area and negative responses in the periphery. As shown in Fig. 18(B)-(ii) and C-(ii), only one side of the triangle matching the preferred orientation is extracted, and a Mach band-like effect is seen clearly around the side, while the other sides are blurred.

V. Conclusion and Discussion

In this paper, a multichip silicon retina composed of the photoreceptor network chip and the horizontal cell network chip was fabricated. The analog outputs of the P chip were transferred to the H chip through a line-parallel data transfer bus. The multichip silicon retina realized a ∇^2G-like receptive field, which carried out smoothing and contrast-enhancement on input images with much higher spatial resolution than that fabricated in our previous study. Furthermore, odd- and even-symmetric oriented filters were obtained in real time by the multichip configuration using external control signals and a simple off-chip subtractor.

In most of the previously fabricated multichips [7]–[13], communication has been realized by AER, in which the spike output of each pixel on the sending array is encoded with a unique address [14], [15], [17]. The AER allows communication between an array of silicon neurons in one chip and another chip, with continuous time spike activity over an asynchronous digital bus [7]; it is better suited for chips employing the continuous time photoreceptor [34], [35]. Therefore, the AER emulates the communication mediated by action potentials and provides a unique methodology for studying the computational advantages with the spike representation. On the other hand, image computations are carried out with analog signals within the retinal circuit. Therefore, the analog data transfer method used in the present multichip naturally emulates the computation of the outer retinal circuit. This analog method is better suited for chips employing the sampled receptor, such as the APS, because the output of the every pixel is read successively and is synchronized with a frame period.

The AER protocol has an advantage of low power consumption. It is more efficient than the analog transfer method when the spike activity in the pixel array is sparse. For example, the motion detection chip and the orientation selective chip fabricated previously consumed only a few milliwatts [7], [9]. The power consumption, however, increases in proportion to the spike activity. It possibly becomes comparable to that of the analog transfer method when the spike activity increases to some extent, since the power consumption can be suppressed in the analog transfer method by supplying the current only to the S/H circuits that are selected by the shift resistor during the data transfer period. Furthermore, the possibility of spike collision also increases in the AER.

Recent digital signal processors can carry out simple preprocessing, such as addition, subtraction, small size mask filtering (3×3 and 5×5 for example), etc., in real-time with low power consumption. The traditional PCs can also carry out the simple preprocessing in real-time but with much higher power consumption. However, it is difficult for these conventional systems to conduct spatial filtering with large size masks that are often required in computation of natural scene [36]. The present multichip realizes large size mask filtering with the resistive networks in real-time with low power consumption. For example, in the even-symmetric filtering, the processing time was about 3.9 ms and the power consumption was about 650 mW. The power consumption will be reduced substantially if the power-saving function is embedded in the present multichip [1]. Furthermore, one can easily design a system consisting of multi-

functional modules to obtain the responses shown in Figs. 10, 14, 16, and 18 in parallel. Therefore, the present multichip architecture is able to combine different image features, i.e., edge, motion, and orientation, etc. [37], in real-time. This system is thought to be applicable to image recognition in which that various different image features are required [38]–[40].

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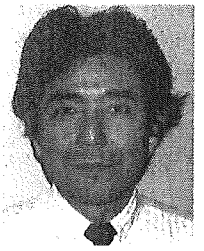

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Flexible and extendible neural interface device based on cooperative multi-chip CMOS LSI architecture

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Abstract

An LSI-based cooperative multi-chip neural interface device, for stimulation as well as recording, is proposed and fabricated. The proposed multi-chip device consists of small (600 μm × 600 μm in the present design) intelligent neural interface unit chips. The unit chip has nine neural stimulation/recording electrodes and an individual control circuit. It can work not only as a stand-alone unit, but also in cooperation with other unit chips. One can configure any number of the unit chips as a multi-chip neural interface device. Compared to conventional single-chip architecture, the proposed multi-chip architecture has a number of advantages including thinness, mechanical strength, flexibility, and extendibility. That makes the multi-chip neural interface device more suitable for in vivo applications than conventional single-chip devices. Packaging technology for the multi-chip device was also developed. We developed a thin, flexible packaging technique for the multi-chip neural interface device and LSI-compatible Pt/Au stacked bump electrodes. The functions of the fabricated multi-chip neural interface device were characterized and the feasibility of the device as a random-access, multi-site stimulator was demonstrated.

Keywords: Retinal prosthesis; Neural interface; Multi-chip; CMOS; Biosensor

1. Introduction

Neural stimulation/recording electrode technology plays an essential role in neuroscience and neuroengineering. The quality and reliability of the neural stimulation/recording strongly depends on the electrode. Various types of electrodes and electrode arrays designed for specific purposes are commercially available, and there has been continuous ongoing development of new electrodes [1–10].

Recently, an increasing number of studies on the development of LSI-based neural interface devices have been reported [11–21]. Since LSI devices can handle electricity with a high integration density, the development of LSI neural interface devices is attracting significant interest, and expectations for performance are high. LSI-based neural interface devices are expected not only for in vitro, but also for in vivo applications. We have been developing retinal prosthesis devices based on CMOS vision chip technology [22–27]. The present research aims to develop an implantable visual prosthesis device that electrically stimulates the retinal neural network with a visual recovering image generated by an intelligent image sensor (vision chip). There is a severe technical issue to overcome in order to apply LSI-based neural interface devices to in vivo neural applications such as retinal prosthesis. For in vivo applications, the device needs to be thin and flexible to fit the physical shapes of target biological neural systems and to avoid damaging the tissues. However, Si, the material of LSI chips, is so rigid that thinning of the LSI chips increases the risk of breakage of the chips. We have previously demonstrated that a Si image sensor chip thinner than 50 μm can be bent, and can work with a sufficient accuracy [25]. However, very careful handling of the LSI chip is required. To overcome the issue of mechanical

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rigidness and realize a feasible LSI-based neural interface device, we have proposed a device architecture consisting of small unit chips that cooperatively work under a single set of control signals [27]. In the present work, we have designed and fabricated an LSI-based cooperative multi-chip neural interface device. The main target application of the device is 2D patterned retinal stimulation. However, the device can be applied not only to retinal prosthesis, but also for various in vivo and in vitro research investigations and applications. We have developed packaging techniques that yield a thin and flexible multi-chip neural interface device for in vivo applications. We have characterized the basic properties and we demonstrate feasibility of the fabricated multi-chip interface device.

2. Concept of cooperative multi-chip neural interface device

Fig. 1 shows the concept of the present multi-chip neural interface device. It has a function to connect any one of the electrodes on the device to an external neural interface line (noted as STIM/REC line, in the present work). The neural cell can be stimulated or the potential sensed via the selected electrode. The multi-chip device consists of an array of small, interconnected unit chips. Each of the unit chips has a neural stimulation/recording electrode array and its own control circuit. A unit chip is controlled via a small number of control lines and can work as a single-chip neural interface device with nine electrodes even in standalone. Once the unit chips are connected to the same set of control lines, they work cooperatively. Cooperative operation is realized in the following way. Each of the unit chips has its own identification address. Every unit chip interprets the control signal that specifies an electrode on one of the unit chips. The unit chips individually determine whether it is selected or not. Only one of the cooperatively working unit chips is enabled and the selected electrode on the selected unit chip is connected to the neural interface line (STIM/REC). In static stimulation/recording mode, one electrode on the selected unit chip is continuously used. The device can be driven in a scanning neural stimulation/recording mode too. Since the typical switching transition time of the LSI devices (at least shorter than 1 μs) is far higher than the response speed of neural cells and the decay time of current injection, it is possible to carry out 2D scanned stimulation or recording of the neural system.

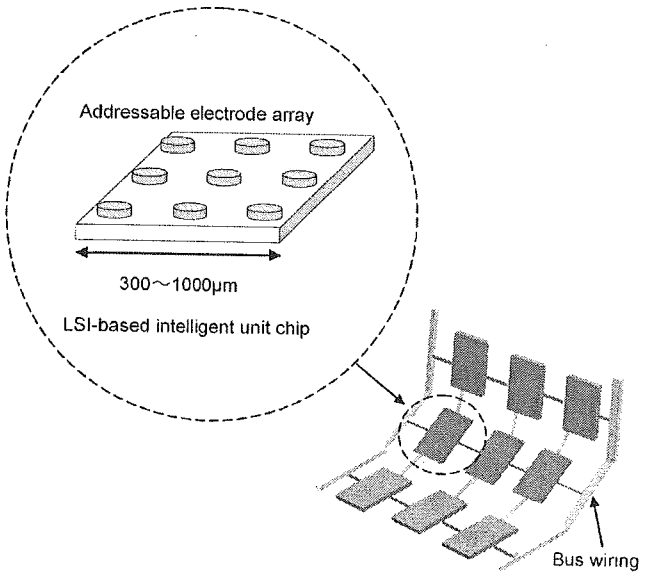


Fig. 1. Concept of the LSI-based multi-chip neural interface device.

Compared with conventional single-chip architecture, the cooperative multi-chip architecture has the following advantages.

2.1. Advantage 1: mechanical strength and flexible packaging

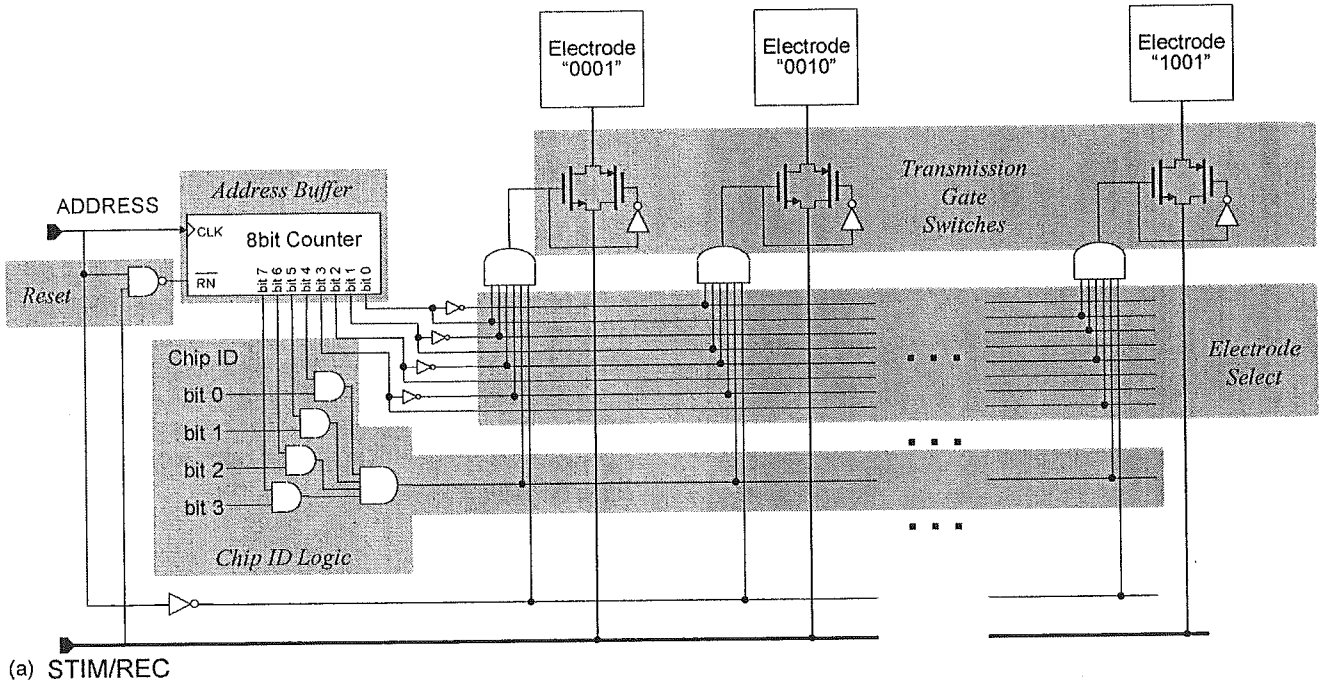
When the thickness of an LSI chip is reduced below 100 μm, the LSI chip can be easily broken by a bending stress. Such fragile LSI-based neural interface chips thus cannot be used for in vivo applications. The straightforward way to improve the mechanical strength of thinned LSI chips is to reduce the chip size. If the chip size is reduced to around 500 μm, it can be handled without any special care to avoid breaking. With the cooperative multi-chip device architecture, the proposed neural interface device has the advantage of reduced risk of crashing. The multi-chip architecture not only has the advantage of mechanical strength of the unit chip, but also an advantage in terms of flexibility in the device packaging. A flexible multi-chip neural interface device can be fabricated by assembling the cooperating unit chips on a flexible substrate with appropriate spacing between the chips. The device can be bent between the unit chips and it is also possible to fabricate a curved device. The techniques for device packaging are described in Section 4.

2.2. Advantage 2: extendibility

In the cooperative multi-chip architecture, the circuitry of the individual unit chips are identical except for the chip identification address which is imprinted as wired memory (in this work). Any of the unit chips can cooperatively work with any other unit chip as long as their identification addresses are different. This makes the configuration of the multi-chip device very flexible. One can configure any number of the unit chips as the multi-chip device. For instance, in the present work, we implemented a 4-bit address space to specify the unit chip. The 4-bit address space means that 16 unit chips can be configured together as a multi-chip neural interface device. Furthermore, the restriction of the address conflict can be overcome by using additional control lines, as described in the next section.

3. Design and functions of the LSI chip

Fig. 2 shows the circuit diagram and the layout of the unit chip used in this study. The chip is designed with 0.6 μm 2poly 3metal standard CMOS technology. The size of a unit chip is 600 μm × 600 μm. This size enables the unit chip to be thinned down to less than 100 μm without a high risk of breaking. The unit chip has nine stimulation/recording electrodes and control circuits. The addresses of the nine electrodes range from "0001" to "1001". Since conventional LSI wiring technology was used to interconnect the unit chips, the wiring pitch needs to be 100 μm or larger. So we should design the function of the device to be quite simple and the number of input/output (I/O) lines must be as small as possible. In the present work, we realized the proposed function with four lines: VDD, GND, ADDRESS, and STIM/REC. As shown in Fig. 2, the unit chip has two terminals for each line. The two terminals assigned to the same signal are connected



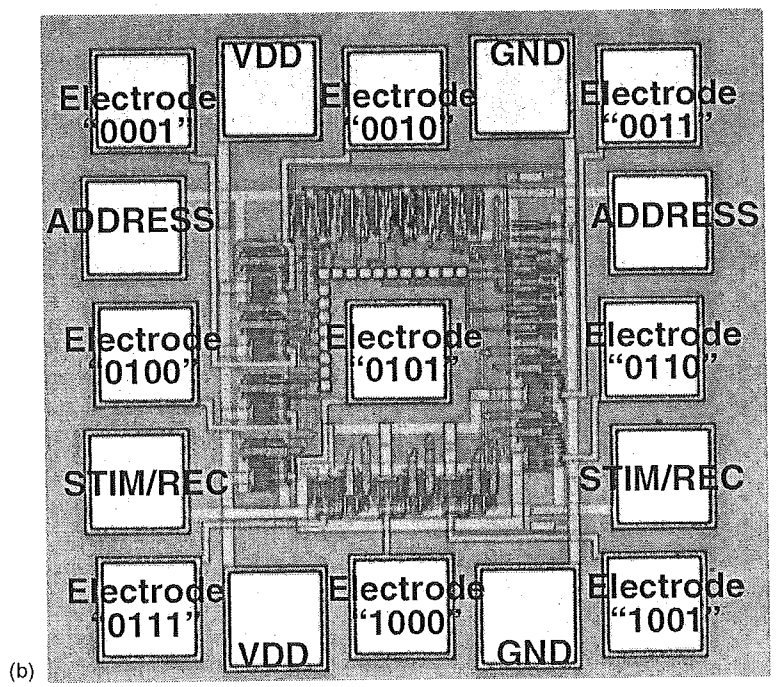


Fig. 2. (a) Circuit diagram and (b) layout of the unit chip.

on the chip directly. Due to this design, the unit chip can relay signals to its nearest neighboring chips and the multi-chip device can be assembled without any crossed wires.

The unit chip has an 8-bit asynchronous counter as an address buffer. The addressing counter counts the digital pulses applied to the ADDRESS line, and the unit chip interprets the value in the counter as the address of the selected electrode. The upper 4-bit and the lower 4-bit represent the addresses of the selected chip and the selected electrode, respectively. Only the selected electrode on the selected chip is connected to the STIM/REC line. Once selected, the neural stimulation/recording can be carried out at the selected electrode via the STIM/REC line. As shown in Fig. 2(a), we adopted a transmission-gate circuitry as the electrode switch. The transmission gate is suitable for the present device which is required to cover the whole voltage region of 0–5 V and the both current direction. Since the address space of the unit chip is 4-bit, 16 unit chips can be controlled by one ADDRESS line. However, we should emphasize that the 4-bit address space does not restrict the number of the unit chips to 16. One can extend the number of integrated unit chips at a cost of just one additional ADDRESS line for every 16 unit chips. Furthermore, we are also developing a multi-chip system with serial interface connections [27].

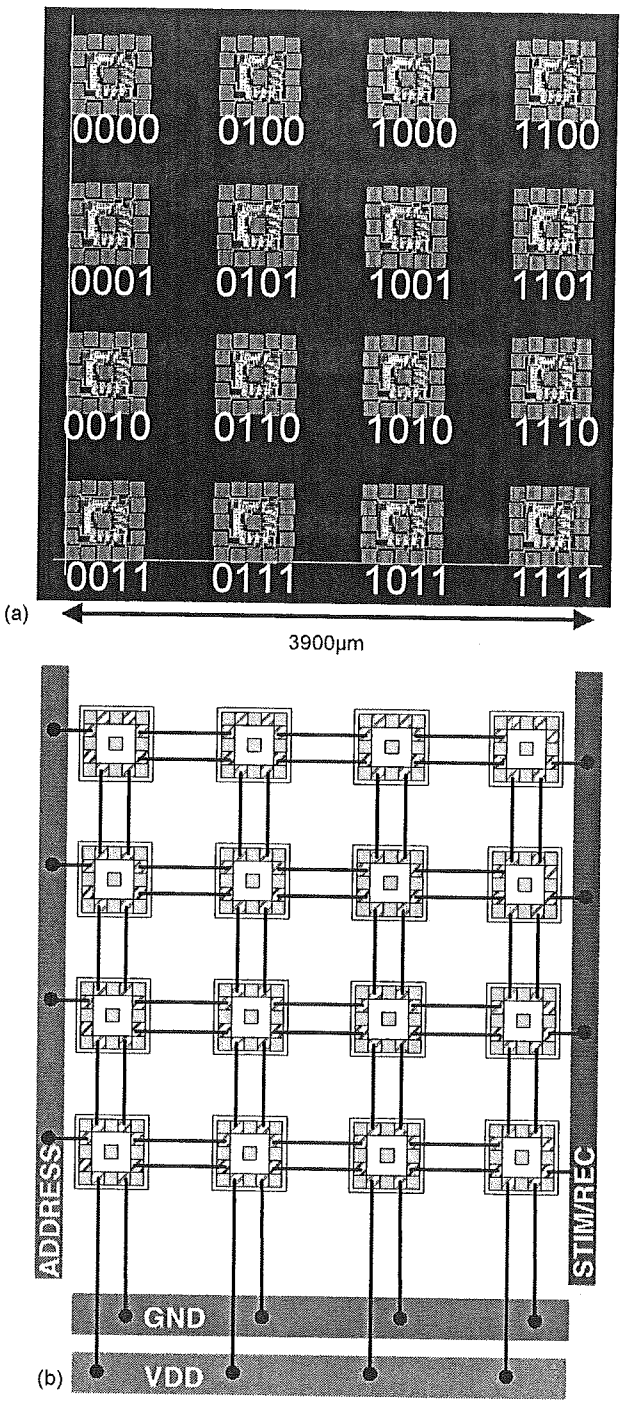


Fig. 3. (a) Layout of the designed LSI die including 4 × 4 unit chips, and (b) connection diagram of a cooperative 4 × 4 multi-chip neural interface device.

In the actual device design, we configured a set of 16 unit chips with different identification addresses on a single LSI die as shown in Fig. 3(a). Thus, the LSI die includes 16 aligned unit chips with binary addresses ranging from "0000" to "1111". The LSI die can be conveniently transformed into a thin, flexible multi-chip neural interface device, as described in the next section. The connection diagram to configure a 4 × 4 multi-chip neural interface device with the default alignment is shown in Fig. 3(b).

4. Packaging technologies for the multi-chip device

In addition to the design of the LSI chips, packaging of the chips is also an important issue to realize a feasible LSI-based neural interface device. A highly reliable molding that separates the bio- and electronic-environments is required. A biocompatible electrode array is also required as the interface between the electronic circuits and neural systems. With the cooperative multi-chip architecture described, the small size of the unit chip (600 μm × 600 μm, in the present design) improves its mechanical strength when thinned. The unit chips aligned on a flexible substrate with appropriate spacing makes the multi-chip device mechanically flexible.

We have been developed packaging technologies for LSI-based neural interface devices. Fig. 4 shows an assembled multi-chip device. Here, a set of 3 × 4 unit chips with addresses from "0000" to "1011" is assembled on a flexible polyimide substrate. The unit chips are wired to each other with Al wires. The chips and Al wires were molded with epoxy resin, except for the top part of the stimulation/recording electrodes. So far, the mold has been confirmed to be resistant to biological environments for acute applications. The molding material needs to be chosen appropriately for specific applications. Although we used Al wires for the interchip connections, Au wiring is also available for chronic applications.

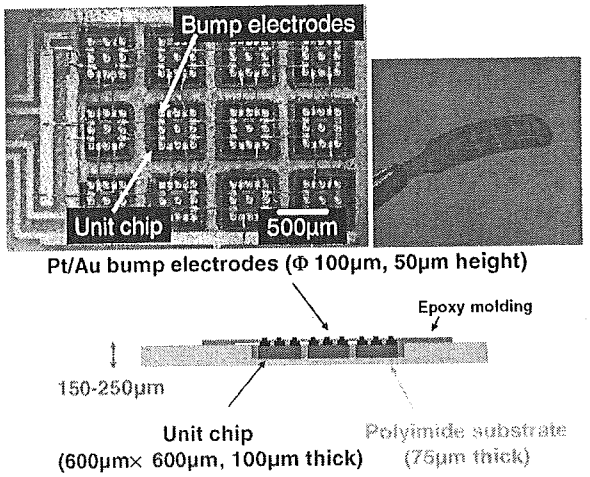


Fig. 4. Packaging of the multi-chip neural interface device.

We have also developed a highly reliable bio-interface electrode array. We improved the bump forming technology, which was originally developed for Au bump forming. We succeeded in forming not only Au, but also Pt bumps using boll bonding/bump forming equipment. Fig. 5 shows a SEM micrograph of Pt/Au stacked electrode array fabricated on an LSI-based neural stimulation device. The lower Au bump of the electrode is used as an intermediate layer because it is difficult to make Pt bump electrodes directly on LSI chips. The Au bump is molded and the electrodes work as bulk Pt electrodes. The typical diameter and height of the electrodes are 100 and 50 μm, respectively. It is to be noted that these bump electrodes can be used not only as bulk Pt electrodes, but also as the core of other high-efficiency bio-compatible electrodes such as IrO_x or TiN [28,29].

As mentioned above, in the present study, we designed a set of 16 unit chips with different identification addresses on a single LSI die (Fig. 3(a)). The unit chips are separated and transferred onto a flexible substrate, maintaining their mutual alignment. The design provides great convenience and reliability for the assembly process. Fig. 6 shows the assembly process flow for a thin, flexible multi-chip neural interface device. At first, grooves with a depth larger than 100 μm were formed on the Si LSI die by micromachining using an excimer laser. The LSI die was attached to a jig with wax, and ground to a thickness of 50–100 μm. The 16 unit chips were separated with the grooves, maintaining their mutual alignment. After a cleaning process, disused chips were removed from the jig, according to the assembly plan of the multi-chip device. The unit chips were glued onto a flexible polyimide substrate using a thermosetting epoxy resin. During the thermosetting process, the wax melted and the unit chips were transferred to the polyimide flexible substrate while maintaining their alignment. The surfaces of the unit chips were cleaned, and Pt/Au bump electrodes and Al wiring were formed. The device was molded with the epoxy resin in the last step. The thickness of the epoxy resin needs to be controlled to only expose the top Pt part of the Pt/Au bump electrodes. The thickness of the assembled device is 150–250 μm, so far.

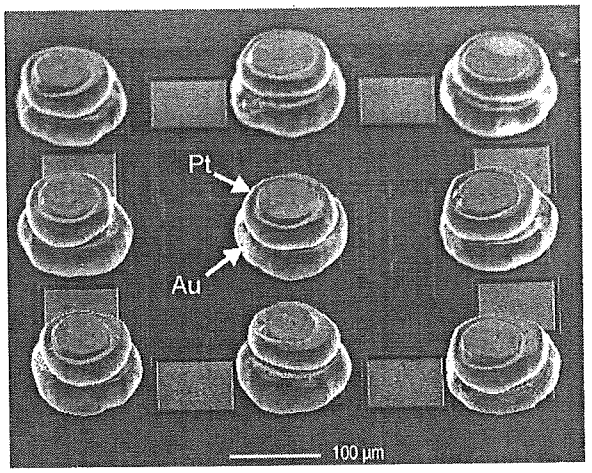


Fig. 5. Pt/Au stacked bump electrode array fabricated on an LSI-based neural stimulation chip.

As shown in Fig. 4, the device can be bent. The maximum curvature will be improved in the future with further optimization of the structure and the assembly process of the device. The risk of breaking the Si chips is far less than for the conventional single-chip architecture. One does not need to take any special care in handling the device, either in the assembly process or during use.

5. External control circuit and device operation

Fig. 7 shows a block diagram of an external control circuit and an example of operational sequence of the multi-chip device. The control sequence consists of three parts: start-up, stimulation/recording, and address change phases. At first, all inputs and the level of the reference electrode (V_{ref}) should be set to 0 V. On applying 5 V to the VDD line, the chips start to operate. After the chips have started, the external circuit resets the unit chips and selects an electrode. In this start-up phase, the STIM/REC signal is also used as a control input. All the unit chips were reset when both the ADDRESS and the STIM/REC were pulled up to the "H" (high) level (higher than 3 V, normally 5 V). Since the STIM/REC line is disconnected from the electrode when the ADDRESS line is "H", we can use the STIM/REC line for the reset trigger. Subsequent to the reset, the external circuit applies a pulse train to the ADDRESS line to select an electrode on the multi-chip device. The selected electrode is connected to the STIM/REC line when the ADDRESS input is "L" (low) level (lower than 2 V, normally 0 V) via a transmission-gate switching circuit. One can either inject current from STIM/REC line to the selected electrode, or sense the potential at the selected electrode through the STIM/REC line.

Due to the circuit configuration of the transmission gate, the voltage range should be between $GND - V_{diff}$ and $VDD + V_{diff}$, where GND and VDD are 0 and 5 V, respectively, in the present work, and V_{diff} is the diffusion

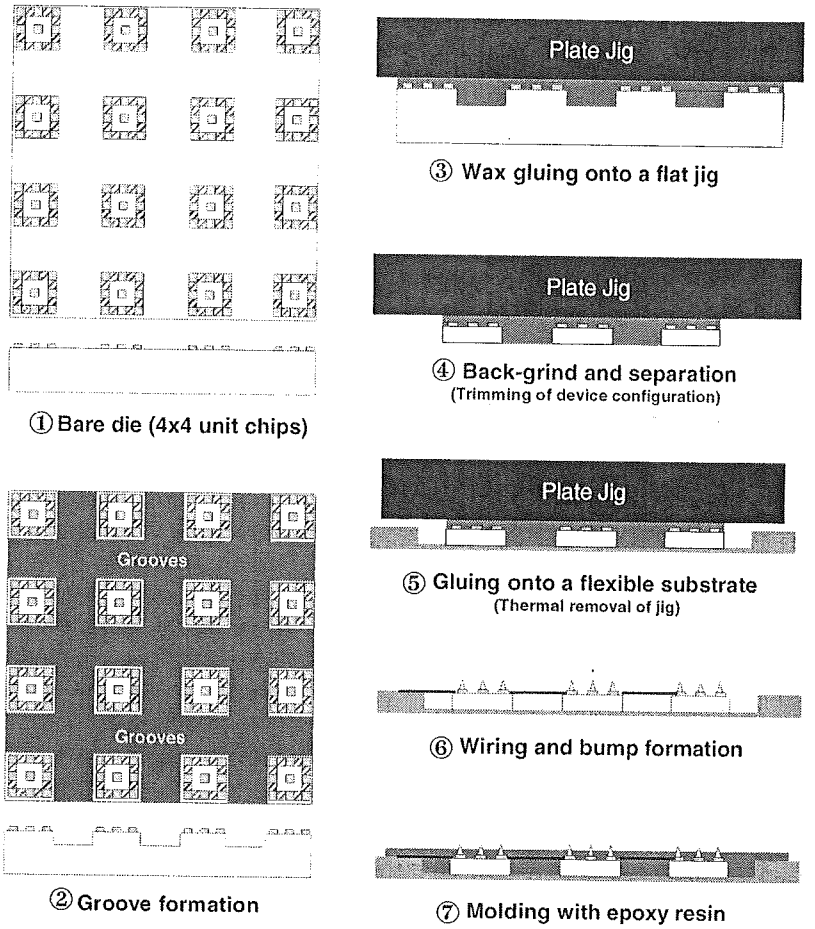


Fig. 6. Assembly process of the multi-chip neural interface device on a flexible polyimide substrate.

potential of Si PN junctions (0.5–0.6 V). The voltage of the STIM/REC line should be maintained between −0.5 and +5.5 V approximately. If the signal voltage exceeds this voltage range, the current flows from the STIM/REC line to GND or VDD to keep the STIM/REC voltage within the operational voltage range. This is a limitation on the voltage swing. However, this characteristic can be used as a safety current bypassing mechanism to avoid any critical damage to biological tissue.

It is generally accepted that neural stimulation should be performed with biphasic current-controlled pulses to maintain the charge balance of the biological environment [15,30]. To use the multi-chip device as a stimulator head, it should be able to handle such biphasic, current-controlled pulses. Therefore, V_{ref} should be set to maintain the equilibrium (zero-current) voltage level of the selected electrode and the STIM/REC line at an intermediate level between −0.5 and 5.5 V for a bidirectional voltage swing. Furthermore, to avoid unintentional reset in address increment for electrode change, the zero-current level must be kept lower than the threshold voltage of the logic circuits (2 V). In actual device operation in a biological environment, a voltage offset appears between V_{ref} and the zero-current level. This offset is discussed in the next section.

6. Characteristics of the fabricated multi-chip neural interface device

To confirm that the addressing function works correctly, we performed a one-by-one pulse transmission test. The 16 unit chips were wired as shown in Fig. 3(b). The input sequence is shown as the upper two traces in Fig. 8. The first pulses applied on both the ADDRESS and the STIM/REC traces are the startup reset command. Subsequently, pulses are alternatively applied on the STIM/REC and ADDRESS lines. Since a pulse on the ADDRESS line increments the address buffers on the unit chips, each pulse applied on the STIM/REC line is relayed to different electrodes. The lower three traces show the signals observed at the electrodes. Trace (a) and (b) are outputs from the first (address: 0001) and second (address: 0010) electrodes on the first unit chip (address: 0000). Trace (c) is the output from electrode 0001 on the unit chip 0001. The pulse applied to the STIM/REC line was relayed to the electrode 00000001 (the electrode "0001" on the chip "0000") immediately after the first pulse was applied on the ADDRESS line. The second pulse on the STIM/REC line was observed not on trace (a), but on (b). This is due to the address increment pulse applied between these two pulses. Then, the STIM pulse was observed on the electrode

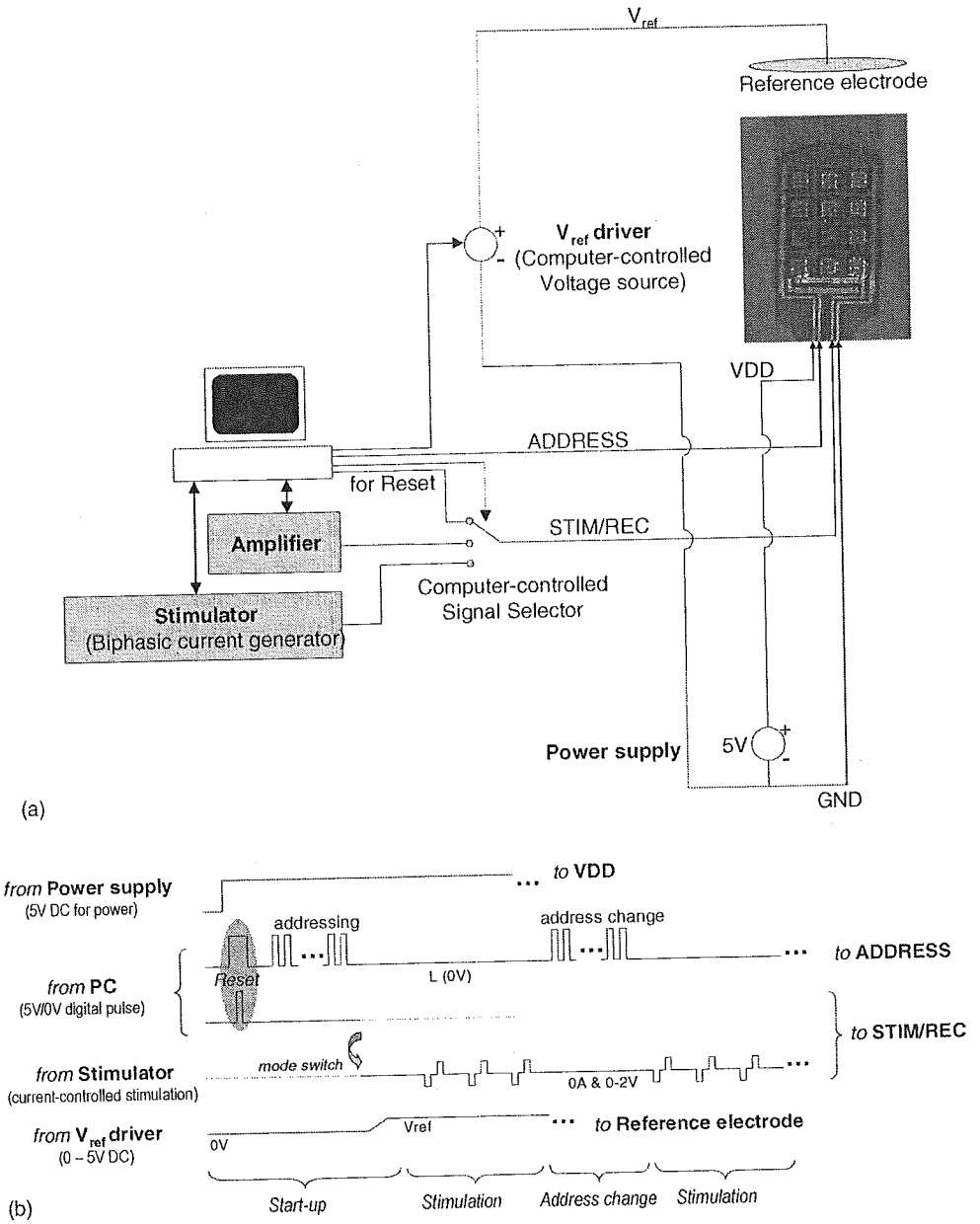


Fig. 7. (a) Block diagram of the external control circuit and (b) an example of control sequence.

"0001001" (the electrode "0001" on the chip "0001") just after the 17th pulse was applied to the ADDRESS line (trace c)). These results show that the addressing function correctly works in the multi-chip configuration. This experiment was carried out with dummy loads of 10 kΩ for each electrode. Crosstalk signals observed on unselected electrodes were smaller than 10 mV. This small signal corresponds to a crosstalk rejection larger than −50 dB. We confirmed that the address increment can be completed within 100 ns, even in the worst case. This means that any electrode can be selected within 26 μs.

Fig. 9 shows the serial resistances R_{series} between the STIM/REC line and the selected electrode. Since the switching circuit is not a mechanical switch, but an electrical

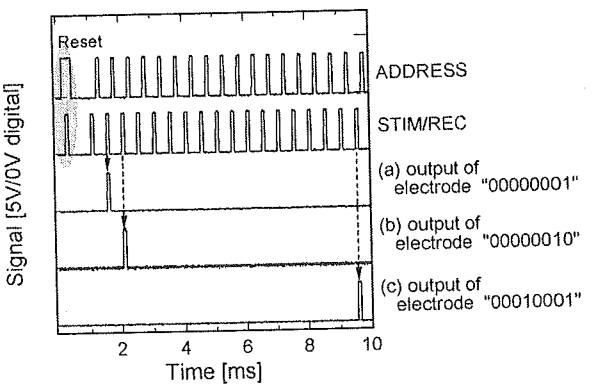


Fig. 8. Addressing function of the multi-chip neural interface device.

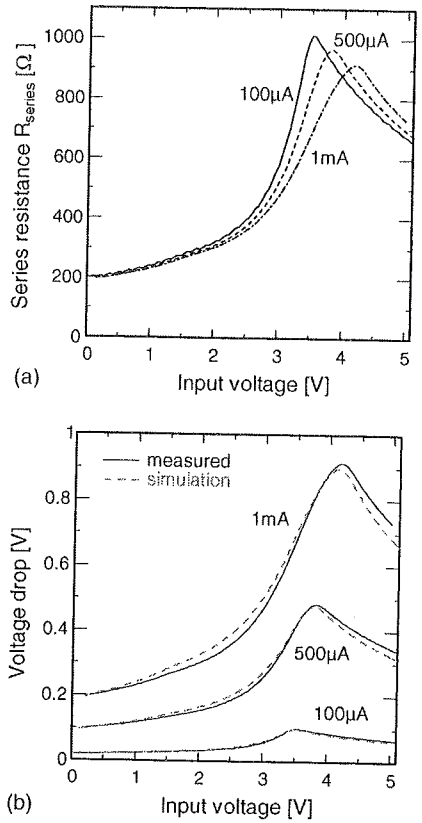


Fig. 9. (a) Series resistance and (b) voltage-drop as a function of the input voltage level.

switching circuit, R_{series} depends on the operational voltage. The series resistance between the STIM/REC line and the selected electrode causes a voltage-drop in the neural stimulation operation, and noise origin in potential measurement operation. The major part of the series resistance is attributed to the on-resistance of the transmission-gate circuit. The voltage-drop V_{drop} is estimated from R_{series} and I (current) using Ohm's law:

$$V_{drop} = R_{series} I$$

Voltage-drops for three typical currents were plotted with simulated results in Fig. 9(b). Since R_{series} is smaller than 1 kΩ, the maximum voltage-drops are smaller than 101 mV, 483 mV, and 915 meV, respectively, for stimulation currents of 100 μA, 500 μA, and 1 mA. These values are not negligible, but are acceptable, because the voltage swing for the current injection in the present work is smaller than 4.0 V. The thermal noise power spectral density S_n (V^2/Hz) of the R_{series} is estimated as follows:

$$S_n = 4kTR_{series}$$

where k is the Boltzmann constant (1.3807×10^{23} J/K) and T is the temperature (K). Assuming the bandwidth for potential sensing operation to be 0–1 MHz, the noise level is estimated to be 4.07 μV or less which is acceptable in potential measurement operations.

We have also characterized the current injection capability of the device in a saline solution. Pt/Au stacked bump electrodes were formed and the chip was molded. Only the top Pt part of the electrodes was exposed with a diameter of approximately 20 μm. The molded chip was dipped in the saline solution and V_{ref} was supplied via an Ag/AgCl reference electrode. The reference voltage was set to 2.5 V and the zero-current voltage was 1.8 V for the present experiment. The voltage mismatch between the operating voltage (1.8 V) and the reference voltage (2.5 V) can be mainly attributed to the difference between the standard potentials in an aqueous solution of Ag/AgCl (0.22 V) and Pt, Pt/$PtCl_x$ (1.2 and 0.73–0.76 V, respectively) [31]. The polarity of the offset between V_{ref} and the zero-current voltage depends on the electrochemical condition at the surface of the electrodes, the past current profile, and the offset current of the stimulator. We measured the voltage traces observed on the STIM line, monitoring whether the current was properly injected. Fig. 10(a) shows the measured operational voltage for typical biphasic, current-controlled pulses. In this work, we chose the same amplitude for cathodic and anodic pulses. The pulse durations of the cathodic and anodic pulses, and the pulse interval between the cathodic/anodic pulses were set to the same value. Hence, the biphasic pulse waveform can be described with just the amplitude and interval such as 100 μA/100 μs, 200 μA/100 μs, 100 μA/200 μs, etc. Similar reports on neural stimulation using Pt electrodes suggest that the trace presented in Fig. 10(a) is reasonable for cathodic-first, biphasic charge injection [32,33]. The nonlinear features observed in Fig. 10(a) are due to electrochemical charge transfer at the electrode surface. Reversible oxidation and reduction of Pt–H and PtO occurs at the interface of the Pt electrode. Furthermore, current injection for charging electrochemical double layer formed in the solution is included in the process at the electrode surface [33]. Fig. 10(b) shows the voltage swing as a function of pulse duration with a fixed pulse height of 100 μA (cathodic)/100 μA (anodic), and Fig. 10(c) shows the voltage swing as a function of pulse height in the case where the pulse duration was fixed at 100 μs (cathodic)/100 μs (interval)/100 μs (anodic). Here, following criteria should be fulfilled to apply the device for neural stimulation such as retinal prosthesis.

From the viewpoint of the voltage range of the LSI, the operational voltage needs to be within the voltage swing of the chip (from −0.5 to +5.5 V for the present device), as shown in the previous section. Fig. 10 shows that the operational voltage is within the voltage range. Since the conditions of the applied pulses are within the range of some typical neural stimulation experiments, we can conclude that the device can be applied for neural stimulation. There is another limitation based on the electrochemical aspect of the current injection into a biological environment. The current injection process from an electrode into saline (or other biological solutions) includes electrochemical reactions at the interface. Excess voltages applied to the interface cause irreversible chemical reactions such as electrolysis or the production of bubbles